-P.E.S. COLLEGE OF ENGINEERING, MANDYA

(AN AUTONOMOUS INSTITUTION AFFILIATED TO VTU, BELAGAVI)

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEM

SCHEME AND SYLLABUS

2024– 25

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

P.E.S COLLEGE OF ENGINEERING, MANDYA-571401

KARNATAKA

Vision

PESCE shall be a leading institution imparting quality engineering and management education developing creative and socially responsible professionals.

Mission

- Provide state of the art infrastructure, motivate the faculty to be proficient in their field of Specialization and adopt best teaching-learning practices.
- Impart engineering and managerial skills through competent and committed faculty using Outcome based educational curriculum.
- Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the societal needs.
- Promote research, product development and industry-institution interaction.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

About the Department:

The department of Electronics and Communication Engineering was incepted in the year 1967 with an undergraduate program in Electronics and Communication Engineering. Initially program had an intake of 60 students and presently 150 students graduate every year. The long journey of 50 years has seen satisfactory contributions to the society, nation and world. The alumni of this department have strong global presence making their alma mater proud in every sector they represent.

Department has started its PG program in the year 2012 in the specialization of VLSI design and Embedded systems. Equipped with qualified and dedicated faculty, department has focus on VLSI design, Embedded systems and Image processing. The quality of teaching and training has yielded high growth rate of placement at various organizations. Large number of candidates pursuing research programs (M.Sc/Ph D) is a true testimonial to the research potential of the department.

Vision

The department of E & C would endeavour to create a pool of engineers who would be **extremely competent technically, ethically strong** also fulfil their obligation in terms of **social responsibility**.

Mission

- **M1:** Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience conducive to imbibe technical knowledge and practicing ethics.
- **M2**:Group and individual exercises to inculcate habit of analytical and strategic thinking to help the students to develop creative thinking and in still team skills
- **M3**:MoUs and Sponsored projects with industry and R & D organizations for Collaborative learning.
- **M4**: Enabling and encouraging students for continuing education and moulding them for life-long learning process.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(A) Programme Learning Objectives (PLOs)

M.Tech in VLSI Design and Embedded system during two years term, aims to

1. Provide the students with strong fundamental and advanced knowledge in VLSI design and Embedded system with an emphasis to solve engineering problems.
2. Train the students in VLSI and Embedded system design tools and make them fit for the industries.
3. Inculcate in students the professional and ethical attitude, effective Communication skills, team spirit and nurture them as leaders.
4. Provide teaching skills and inculcate spirit of research.
5. Motivate to continue education leading to doctoral degree and choose research as Career option.

(B) Programme educational outcomes

The objectives aim to produce qualified Electronic Engineering Post-graduates who will:

PEO 1: Identify and apply appropriate Electronic Design Automation (EDA) tools to solve real world problems in VLSI and Embedded Systems domain so as to create innovative products and systems.

PEO 2: Develop managerial skill and apply appropriate approaches in the domain of VLSI design and Embedded Systems incorporating safety, sustainability and become a successful professional or an Entrepreneur in the domain.

PEO 3: To exhibit professional competence and leadership qualities with harmonious blend of ethics leading to an integrated personality development.

(C) Programme Outcomes (POs):

The Master of Technology Programme in Electronics and Communication Engineering [M.Tech in VLSI Design and Embedded systems] must demonstrate that its Post graduates have

PO1: Ability to solve multidisciplinary problems using VLSI circuits in multiple ways and provide optimized solutions.

PO2: Demonstrate a degree of mastery over the area of VLSI Design and Embedded Systems. The mastery should be a level higher than the requirements of the bachelor's in electronics &communication engineering program.

PO3: Ability to use techniques and modern CAD tools so as to implement them in engineering practice to develop professional skills that will prepare the students for immediate employment in the relevant branch of engineering in industry.

PO4: Acquire professional and intellectual integrity, research ethics and execute socio-concern projects related to modern VLSI and embedded systems

PO5: Write and present a substantial technical report/document in the field of VLSI design and embedded systems

Program Specific Outcomes:

PSO-1: An ability to understand the basic concepts in VLSI DESIGN AND EMBEDDED SYSTEMS and to apply them in the design and implementation of VLSI AND EMBEDDED CIRCUITS

PSO-2: An ability to solve complex problems in VLSI DESIGN AND EMBEDDED SYSTEMS, using latest hardware and software tools, along with analytical skills to arrive at appropriate solutions.

I – Semester										
Sl. No.	Course Type	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	CIE	SEE	Total	
				L	P	T/SDA				
1.	IPCC	P24MECE11	System Verilog	3	2	0	50	50	100	4
2.	PCC	P24MECE12	Advanced Machine Learning and Deep Learning	3	0	0	50	50	100	3
3.	PCC	P24MECE13	Digital Circuits and Logic Design	3	0	0	50	50	100	3
4.	PEC	P24MECE14X	Professional Elective I	3	0	0	50	50	100	3
5.	PEC	P24MECE15X	Professional Elective II	3	0	0	50	50	100	3
6.	PCL	P24MECEL16	VLSI Design Lab	0	1	1	50	50	100	2
7.	NCMC	P24MRMI17	Research Methodology and IPR(**Online**)		Online courses(online.vtu.ac.in)					PP
Total							**300**	**300**	**600**	**18**

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses |PEC- Professional Elective Course| NCMC-Non Credit Mandatory Course | PECL - Professional Elective Lab

Professional Elective - I			Professional Elective - II		
Sl. No	**Course Code**	**Course Title**	**Sl. No**	**Course Code**	**Course Title**
1.	P24MECE141	ASIC Design	1.	P24MECE151	Advance Embedded Systems
2.	P24MECE142	Advanced Computer Networking	2.	P24MECE152	Advanced Wireless Communication
3.	P24MECE143	Advanced Signal Processing	3.	P24MECE153	Multimedia and Applications
4.	P24MECE144	Power Converters	4.	P24MECE154	Process Control

II – Semester										
Sl. No.	Course Type	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	CIE	SEE	Total	
				L	P	T/SDA				
1.	IPCC	P24MECE21	Design of Analog and Mixed Mode VLSI Circuits	3	2	0	50	50	100	4
2.	PCC	P24MECE22	VLSI Testing & Verification	3	0	0	50	50	100	3
3.	PCC	P24MECE23	ARMCortex-M3andM4Processors	3	0	0	50	50	100	3
4.	PCC	P24MECE24	Real time operating Systems	3	0	0	50	50	100	3
5.	PEC	P24MECE25X	Professional Elective III	3	0	0	50	50	100	3
7.	PEC	P24MECE26X	Professional Elective IV	3	0	0	50	50	100	3
8.	PCL	P24MECML27	VLSI Design & Embedded Systems Lab	0	1	1	50	50	100	2
9	AEC/SEC	P24MECEL28	Ability/Skill Enhancement Course (Offline/Online)	1	-	-	50	50	100	1
Total							**400**	**400**	**800**	**22**

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses |PEC- Professional Elective Course| NCMC-Non Credit Mandatory Course | PECL - Professional Elective Lab

Professional Elective - III			Professional Elective - II		
Sl. No	Course Code	Course Title	Sl. No	Course Code	Course Title
1.	P24MECE251	FinFETs and Other Multi-Gate Transistors	1.	P24MECE261	Reconfigurable Computing
2.	P24MECE252	Hardware Security	2.	P24MECE262	Long Term Reliability of VLSI Systems
3.	P24MECE253	Static Timing Analysis	3.	P24MECE263	Low Power VLSI Design
4.	P24MECE254	Embedded Linux System Design and Development Processing	4.	P24MECE264	RISC V

III – Semester										
Sl. No.	Course Type	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	CIE	SEE	Total	
				L	P	T/SDA				
1.	PEC	P24MECE31X	(Online Courses)12weeksduration				100		100	3
2.		P24MECE32X	(Online Courses)12weeksduration				100		100	3
3.		P24MECE33X	(Online Courses)12weeksduration				100		100	3
4.	INT	P24MECE34	Research Internship/ Industry-Internship leading to project work/ Start up				100		100	3
Total							**400**		**400**	**12**

III – Semester										
Sl. No.	Course Type	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	CIE	SEE	Total	
				L	P	T/SDA				
1.	INT	P24MECE41	Research Internship/ Industry Internship Leading to Project Work/Start-up				100	100	100	12
2.	PROJ	P24MECE42	Project				100	100	100	16
Total							**200**	**200**	**400**	**28**

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **SYSTEM VERILOG**		
Course Code: **P24MECE11**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:2	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3	
Credits:**04**		
Prerequisite:		
Digital Logic Design, Verilog, VLSI Testing and Verification		
Course learning Objectives:		
CLO1:Understand Digital System Verification Using Object Oriented Methods CLO2: Learn the System Verilog Language for Digital System Verification. CLO3: Create/Build Test Benches for the Design/Methodology. CLO4: Use Constrained Random Tests for Verification CLO5: Understand Concepts of Functional Coverage		
UNIT -1		8 Hours
Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench. **Data Types**: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With type def, Creating User Defined Structures, Type Conversion, Enumerated Types, Constants and Strings, Expression Width.		
Self-Study Content: Analyse the Difference between Verilog and System Verilog Data types		
Textbook Map: Chapter-1 : 1.1,1.3-1.10 Chapter-2 : 2.1-2.9, 2.11,2.13-2.16		
Teaching Learning Process: PPT,		
UNIT 2:		8 Hours
Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. **Connecting the Test Bench and Design**: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.		
Self-Study Content: Develop a System Verilog Code for Conditional Circuits using Procedural Statements		
Textbook Map: Chapter-3 :3.1-3.7 Chapter 4: 4.1-4.4, 4.9		
Teaching Learning Process: PPT		
UNIT 3:		8 Hours
Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, In Line Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.		
Self-Study Content: Understand the basic OOPs Concepts		
Textbook Map: Chapter-6.1,6.3-6.8,6.10,6.12,6.15,6.16		
Teaching Learning Process: PPT		
UNIT 4:		8 Hours
Threads and Inter process Communication: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, Building A Test Bench with Threads and Inter Process Communication.		
Self-Study Content: Analyse the usage of Inheritance in System Verilog		

Textbook Map: Chapter-7				
Teaching Learning Process: PPT				
UNIT 5:				8 Hours
Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.				
Self-Study Content: Case study of ALU for Functional Coverage				
Teaching Learning Process: PPT				
Textbook Map: Chapter-9				
Course Outcomes: At the end of the course students should be able to :				
CO1: Apply the System Verilog concepts to verify the design. CO2: Apply constrained random tests benches using System Verilog. CO3: Appreciate Functional Coverage				
Suggested Learning Resources:				
Textbooks:				
1.	Title	Author	Year & Edition	Publisher
1	System Verilog for Verification–A guide to learning the Testbench language features	ChrisSpear	Second Edition, 2010	Springer Publications
2	System Verilog for Design-A guide to using system Verilog for Hardware design and modelling	Stuart Sutherland, Simon Davidmann, Peter Flake	Second Edition, 2006	Springer Publications
Reference Books:				
1.	System Verilog for Design	Stuart Sutherland	2nd edition, 2006	Springer Publications
2.	System Verilog Assertions	Vijaya Raghavan	2014	Springer Publications
Web links and Video Lectures (e-resources)				
1.https://www.youtube.com/watch?v=N9cdUhdNrgg&list=PLqPfWwayuBvOL920Q8ljlVmUMHshb5lJE				
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)				
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing				

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **SYSTEM VERILOG**		
Course Code: **P24MECE11**	CIE Marks: 50	CIE Weightage: 50
Teaching hours/week (L:T:P)3:0:2	SEE Marks:100	SEE Weightage:50
Teaching hours of Pedagogy:40	Exam Hours: 3	
Credits: 04		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes:	**Expected Bloom's Level**	**Program Outcomes**
CO1: Apply the System Verilog concepts to verify the design.	L2, L3	PO1, PO3, PO4, PO5
CO2: Apply constrained random tests benches using System Verilog.	L3,L4	PO1, PO4, PO5
CO3: Appreciate Functional Coverage.	L2,L3	PO1,PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3		1	1	2	3	
CO2	2			1	2	2	
CO3	2			1		2	

PRACTICAL COMPONENT OF IPCC **Using simulation software Vivado**	
1.	Develop a System Verilog code to simulate and verify the operation of a tri state buffer.
2.	Using function facilities of SystemVerilog develop a code forgiven arithmetic/logical operation and verify its operation through its test bench simulation.
3.	Using task facility of System Verilog develop a code to synthesize given logical functionality, verify its operation through test bench and also comment on synthesizability with respect to return type.
4.	Using class data types in System Verilog develop a code for control register with given specifications and simulate its operation.
5.	Develop a System Verilog code to illustrate the concept of threads and fork.
6.	Develop a System Verilog code to create semaphores for controlling the register access.
7.	Using randomization facility in System Verilog develop a test bench to verify the operation of a given logic design.
8.	Using Enumerated type facility in System Verilog develop a code to simulate the operation of a traffic control state machine.

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED MACHINE LEARNING AND DEEP LEARNING**		
Course Code**: P24MECE12**	CIE Marks:50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40 hrs	Exam Hours: 03(Theory)	
Credits: **03**		
Prerequisite:		
Basic operating understanding of calculus, matrices and Python programming. And provide extensive mathematical background, in linear algebra may also be helpful in navigating certain sections of mathematical exposition. Knowledge of neural network architecture and design.		
Course Learning Objectives: CLO1: To understand the fundamental concepts of machine learning and its applications. CLO2: To master the concepts of classification and clustering techniques. CLO3: To develop a deep understanding of convolutional neural networks (CNNs) and their architecture. CLO4: To apply deep learning techniques to large-scaled at a sets and real-world problems.		
UNIT -1		8 Hours
The Neural Network: Building Intelligent Machines, Limits of Traditional Computer Programs, Mechanics of Machine Learning, Neuron, Expressing Linear Perceptron's as Neurons, Feed-Forward Neural Networks, Linear Neurons and Their Limitations, Sigmoid, Tanh, and ReLU Neurons, Soft max Output Layers. **Training Feed-Forward Neural Networks**: Fast-Food Problem, Gradient Descent, Delta Rule and Learning Rates, Gradient Descent with Sigmoidal Neurons, Back propagation Algorithm, Stochastic and Mini batch Gradient Descent, Test Sets, Validation Sets, and Over fitting, Preventing Over fitting in Deep Neural Networks. **RBT Levels:** L2, L3		
Self-Study Content:1. Study the basic intuition for machine learning. 2. Discuss the basic structure of a neuron, how feed-forward neural networks works.		
Textbook 1 Map: 1.1 to 1.10 and 2.1 to 2.8		
Teaching Learning Process: Power point presentation with demonstration (MAT LAB or Python) or any violable tool.		
UNIT 2:		8 Hours
Beyond Gradient Descent: Challenges with Gradient Descent, Local Minima in the Error Surfaces of Deep Networks, Model Identifiability, Flat Regions in the Error Surface, When the Gradient Points in the Wrong Direction, Momentum-Based Optimization, Brief View of Second-Order Methods, Learning Rate Adaptation, AdaGrad—Accumulating Historical Gradients, RMSProp—Exponentially Weighted Moving Average of Gradients, Adam—Combining Momentum and RMSProp, Philosophy Behind Optimizer Selection. **RBT Levels:** L3		
Self-Study Content: 1. Identify the challenges that arise when trying to train deep networks with complex error surfaces. 2.Understand how momentum can be used to overcome ill-conditioning.		
Textbook 1 Map: 4.1 to 1.10		
Teaching Learning Process: Power point presentation with demonstration (MAT LAB or Python) or any violable tool.		

UNIT 3:	8 Hours
Convolutional Neural Networks: The operation, Pooling, Convolution and Pooling as an infinitely strong prior, Variants of the basic functions, efficient algorithms, Random or Unsupervised Features, Neuro scientific Basis for Convolutional Networks. **RBT Levels:** L3	
Self-Study Content: 1. Identify the applications of convolution neural networks. 2. Develop a python code for Efficient Convolution Algorithms.	
Textbook 2 Map:9.1 to 9.5, 9.8 to 9.10	
Teaching Learning Process: Power point presentation with case studies and/or demonstration (MAT LAB or Python) or any violable tool.	
UNIT 4:	8 Hours
Neural Networks: RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated Optimization for Long Term Dependencies. **RBT Levels:** L3	
Self-Study Content: 1.Understand the concept of multi-layer networks of Recurrent Neural Networks. 2. Identify the different Long Short Term Memory and other Gated RNNs.	
Textbook 2 Map: 10.2 to 10.6, 10.10 to 10.11	
Teaching Learning Process: Power point presentation and guest lecture.	
UNIT 5:	8 Hours
Applications: Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications. **RBT Levels:** L3,L4	
Self-Study Content: 1. Discuss how to use deep learning to solve applications in computer vision, speech recognition, natural language processing, and other application areas of commercial interest	
Textbook 2 Map: 12.1 to 12.5	
Teaching Learning Process: Power point presentation and seminar.	
Course Outcomes: At the end of the course students should be able to :	
CO1: **Illustrate** the principles and mechanism of working of neural networks. CO2: **Analyze** the effectiveness of neural networks and their architectures in solving a problems. CO3: **Develop** a neural network/machine learning model to solve given problem.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Fundamentals of Deep Learning	Nikhil Budama	2017, 1st Edition	O'Reilly Media, Inc, USA ISBN-10 9781491925614 ISBN-13978-1491925614
2	Deep Learning	Goodfellow, Bengio and Courville	2018	The MIT Press,2016,800 pp,ISBN:0262035618
Reference Books:				
1.	Neural Networks and Deep Learning	CharuAggarwal	2018	
2.	Hands-on Deep	Sudharsan,	2019	

	Learning Algorithms with Python	Ravichandran		

Web links and Video Lectures (e-resources)
1. https://nptel.ac.in/
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title:**ADVANCED MACHINE LEARNING AND DEEP LEARNING**		
Course Code: **P24MECE12**	CIE Marks:50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40 hrs	Exam Hours: 03(Theory)	
Credits: 03		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Illustrate the principles and mechanism of working of neural networks.	L2	PO1
CO2: Analyze the effectiveness of neural networks and their architectures in solving problems.	L3	PO2
CO3: Develop a neural network/machine learning model to solve given problem**.**	L5	PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3			2				

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **DIGITAL CIRCUITS AND LOGIC DESIGN**		
Course Code: **P24MECE13**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P:): 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	

Credits**:03**	
Prerequisite:	
Electric Circuits, Microelectronics, Digital Systems.	
Course learning Objectives:	
CLO1: Understand the concepts of sequential machines. CLO2: Apply fault detection experiments to sequential circuits. CLO3: Analyze the faults in the design of circuits. CLO4: Design Sequential Machines/Circuits	
UNIT -1	8 Hours
Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite-State Model, Further Definitions, Capabilities	
Self-Study Content: State equivalence and machine minimization	
Textbook Map 1: 7.1,7.2 10.1,10.2	
Teaching Learning Process: Poster presentation/Quiz/Seminar/Team demonstration	
UNIT 2:	8 Hours
Testing of Combinational Circuits: Fault models, Structural testing, I_{DDQ} testing, Delay fault testing, Synthesis for testing, Testing for nanotechnologies.	
Self-Study Content: Fault Diagnosis of Digital Circuits	
Textbook Map 1: 8.1, 8.2, 8.3, 8.4, 8.5,8.6	
Teaching Learning Process: Flip class/Quiz/Seminar/Team demonstration	
UNIT 3:	8 Hours
Introduction to Synchronous Sequential circuits and iterative networks: Sequential circuits-introductory example, The finite- state model-basic definitions, Memory elements and their excitation functions, Synthesis of synchronous sequential circuits, An example of a computing machine	
Self-Study Content: Iterative Networks	
Textbook Map 1: 9.1, 9.2, 9.3, 9.4, 9.5	
Teaching Learning Process: Quiz/Seminar/Team demonstration/One minute paper writing	
UNIT 4:	8 Hours
Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.	
Self-Study Content: Built-in self-test (BIST)	
Textbook Map 1: 12.1,12.2,12.3,12.4,12.5,12.6,12.7,12.8,12.9	
Teaching Learning Process: One minute paper writing/ Quiz/Seminar/Team demonstration	
UNIT 5:	8 Hours
Faults in Digital Circuits: Failures and faults, Modelling of faults, Stuck-At-Faults, Bridging faults, Breaks and Transistor Stuck-On/-Open faults in CMOS, Delay faults. **Test Generation for Sequential Circuits:** Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models	
Self-Study Content: Test Generation Based on Functional Fault Models	
Teaching Learning Process: Think pair share/One minute paper writing/ Quiz/Seminar	
Textbook Map 2: 1.1, 1.2, 1.2.1, 1.2.2, 1.2.3,1.2.4, 1.3, 4.1,4.2,4.3,4.4.	
Course Outcomes: At the end of the course students should be able to :	
CO1:Apply electronics circuit knowledge to understand digital circuits. CO2:Analyze digital circuits for faults using various methods.	

CO3: Design the fault detection circuit for synchronous sequential circuits.
CO4:Simulate fault models with available tools.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	'Switching and Finite Automata Theory'	ZviKohavi		ISBN:978_0_07_099387_7 2nd Edition ,2008.
2	'Digital Circuit Testing and Testability'	Parag K Lala		Academic Press

Reference Books:

1.	Digital Circuits and logic Design', Charles RothJr	Parag K Lala	PrenticeHallInc.1985.	
2.	'Introductory Theory of Computer'	E.V.Krishnamurthy	1983	Macmillan PressLtd
3	Fault Tolerant and Fault Testable Hardware Design'	Parag K Lala	1985.	Prentice HallInc.
4	Theory of computer science–Automata, Languages and Computation	Mishra & Chandrasekaran,	2ndEdition, PHI, 2004.	

Web links and Video Lectures (e-resources)

1. https://nptel.ac.in/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **DIGITAL CIRCUITS AND LOGIC DESIGN**		
Course Code: **P24MECE13**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P:): 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03(Theory)	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Apply knowledge of electronics circuit to understand the concepts of digital circuits.	L1	PO1
CO2: Analyse the faults in the digital circuits using various methods.	L2	PO2
CO3: Design the fault detection circuit for synchronous sequential circuits.	L5	PO2
C04: Simulate fault models with available tools.	L5	PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		3					3
CO3		2					2
CO4			2				

PROFESSIONAL ELECTIVE I		
PART A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ASIC DESIGN**		
Course Code: **P24MECE141**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3Hrs	
Credits: 03		
Prerequisite:		
• Basic Semiconductor Concepts. • Digital Logic Design. • HDL (Hardware Description Language). • EDA Tools (Electronic Design Automation). • Simulation and Verification.		
Course learning Objectives:		
CLO1: To learn ASIC methodologies and programmable logic cells to implement a function on IC. CLO2: To analyze back-end physical design flow, including partitioning, floor-planning, placement, and routing. CLO3: To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs		
UNIT -1		8 Hours
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic**: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.		
Self-Study Content: Case Study, Carry out the survey on ASIC ICs which are used in industries.		
Textbook Map: Text 1: 1.1.1,1.1.2,1.1.7, 1.2,1.5,2.6(2.6.1,2.6.2,6.2.3,2.6.4,2.6.6),2.8.		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, ActedACT:ACT1, ACT2andACT3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/OBlock.		
Self-Study Content: Other Data path Operators, Library Architecture, Gate array Design.		
Textbook Map:3.3,3.4,5.1(5.1.3,5.1.4),5.2.1,5.3,5.4,6.7		
Teaching Learning Process: Seminar		
UNIT 3:		8 Hours
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction**: Physical Design, CAD Tools, System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.		
Self-Study Content: Schematic –Entry tools and Back annotation.		
Textbook Map: Text 1: 9.1(9.1.1 to 9.1.11), 15.1,15.2,15.3,15.4,15.7 (15.7.1,15.7.3,15.7.4, 15.7.5,15.7.7)		

Teaching Learning Process: Seminar	
UNIT 4:	8 Hours
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	
Self-Study Content: Introduction to Synthesis and Simulation.	
Textbook Map: Text 1: 16.1,16.2.2,16.2.16.2.4,16.2.6,16.2.8,16.3	
Teaching Learning Process: Paper Presentation	
UNIT 5:	8 Hours
Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	
Self-Study Content: Partitioning methods, Global Routing, Detail Routing, Special Routing.	
Textbook Map: Text1: 17.1(17.1.1,17.1.3,17.1.4,17.1.7), 17.2(17.2.1,17.2.2,17.2.4, 17.2.6, 17.2.7, 17.2.8,17.2.9)17.3,17.4	
Teaching Learning Process: Paper Presentation	
Course Outcomes: At the end of the course students should be able to :	
CO1: Describe the concepts of ASIC design methodology, data path elements, logical effort. CO2: Analyze the design of ASICs suitable for specific tasks, perform design entry and Explain the physical design flow. CO3: Design data path elements for ASIC cell libraries and compute optimum path delay. CO4:Create floor plan including partition and routing with the use of CAD algorithms	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	"**Application - Specific Integrated Circuits**"	M.J.S .Smith	1st Edition, 2003.ISBN-13: 978-8177584080.	Pearson Education
Reference Books:				
1.	**"CMOS VLSI Design: A Circuits and Systems Perspective"**	Neil H.E. Weste, David Harris, and Ayan Banerjee	3rdedition, 2011	Addison Wesley/ Pearson education
2.	**"VLSI Design: A Practical Guide for FPGA and ASIC Implementations"**	Vikram Arkalgud Chandrasetty	ISBN: 978-1-4614-1119-2.2011	Springer
3.	**"An ASIC Low Power Primer"**	RakeshChadha,BhaskerJ,	ISBN:978-14614-4270-7.	Springer
4.	**"Digital Design (Verilog):An Embedded Systems Approach Using Verilog"**	PeterJ.Ashenden	1stEdition	Kindle Edition

Web links and Video Lectures (e-resources)

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **ASIC DESIGN**		
Course Code: **P24MECE141**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3Hrs	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Describe the concepts of ASIC design methodology, data path elements, logical effort.	L1	PO1
CO2: Analyze the design of ASICs suitable for specific tasks, perform design entry and Explain the physical design flow.	L2	PO2,PO3
CO3: Design data path elements for ASIC cell libraries and compute optimum path delay.	L5	PO3
CO4: Create floor plan including partition and routing with the use of CAD algorithms.	L5	PO4
CO5: Design CAD algorithms and explain how these algorithms interact in ASIC design.	L5	PO3,PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	**2**					**2**	
CO2		**2**	**2**				**2**
CO3			**3**				
CO4				**3**			
CO5			**2**	**2**			

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED COMPUTER NETWORKING**		
Course Code: **P24MECE142**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3	
Credits: **03**		
Prerequisite:		
A secure Internet connection from the Internet Service Provider (ISP), A router with a high-speed Internet connection, A modem, Firewall capabilities, One or more switches (allows computers to link to one another over an internal network), Phone line/cable/fiber optic linking (wired or wireless)		
Course learning Objectives:		
CLO1:This course focuses on advanced networking concepts for next generation network architecture and design CLO2:It covers SDN and virtualization for designing next generation networks		
UNIT -1		8 Hours
MEDIUM ACCESS CONTROL SUB LAYER: Wireless LANs, Broadband Wireless, Bluetooth, RFID. THE NETWORK LAYER: Network Layer Design Issues, Congestion Control Algorithms, Quality of Service, The Network Layer in the Internet.		
Self-Study Content: Technical terminology used in Computer Networking and Internet working.		
Textbook Map:(Text Book 1: 4.4, 4.5, 4.6, 4.7,5.1, 5.3, 5.4, 5.6.3 to 5.6.9) (RBT Levels: L1 & L2)		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
THE APPLICATION LAYER: The Domain Name System, Electronic Mail, The World Wide Web.		
Self-Study Content: Recent concepts of Application Layer		
Textbook Map:(Text Book 1: 7.1, 7.2, 7.3) (RBT Levels: L1 & L2)		
Teaching Learning Process: Seminar/ poster Presentation		
UNIT 3:		8 Hours
SOFTWARE DEFINED NETWORK (SDN): Evolution of Switches and Control Planes, Cost, SDN Implications for Research and Innovation GENESIS OF SDN: The Evolution of Networking Technology, Forerunners of SDN, Software Defined Networking is Born, Sustaining SDN Interoperability, Open Source Contributions, Network Virtualization HOW SDN WORKS: Fundamental Characteristics of SDN, SDN Operation, SDN Devices, SDN Controller, SDN Applications, Alternate SDN Methods		
Self-Study Content: Important components of SDN controllers		
Textbook Map: (Text Book 2: 2.1, 2.2, 2.3, 3.1, 3.2, 3.4, 3.5, 3.6, 3.7, 4.1 to 4.6) (RBT Levels: L1 & L2)		
Teaching Learning Process: Individual Role play/Team Demonstration/ Collaborative Activity		

UNIT 4:	8 Hours
THE OPENFLOW SPECIFICATION: Open Flow Overview, Open Flow 1.0 and Open Flow Basics, Open Flow Additions - 1.1, 1.2, 1.3, 1.4, 1.5, Improving Open Flow Interoperability, Optical Transport Protocol Extensions, Open Flow Limitations	
Self-Study Content: Differentiate between SDN and open flow	
Textbook Map:(Text Book: 2 Chapter 5) (RBT Levels: L1& L2)	
Teaching Learning Process: Case study	
UNIT 5:	8 Hours
NETWORK FUNCTIONS VIRTUALIZATION: Definition of NFV, Virtualize, Standards, OPNFV, Leading NFV Vendors, SDN Vs NFV, In-Line Network Functions. SDN OPEN SOURCE: SDN Open Source Landscape, The OpenFlow Open Source Environment, Profiles of SDN Open Source Users, OpenFlow Source Code, Switch Implementations, Controller Implementations, SDN Applications, Orchestration and Network Virtualization, Simulation, Testing and Tools, Open Source Cloud Software, Example: Applying SDN Open Source.	
Self-Study Content: Recent updates & study on physical components of Computer network	
Teaching Learning Process: Learn by Doing	
Textbook Map:(Text Book 2: 10.1-10.7 & 13.1, 13.2, 13.5 - 13.13) (RBT Levels: L1 & L2)	
Course Outcomes: At the end of the course students should be able to :	
CO1: Understand advanced concepts and next generation networks. CO2: Analyze network Algorithm's, Protocols and their functionalities. CO3: Comprehend features of SDN and its application to next generation Systems	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Computer Network	Andrew S. Tanenbaum, David J. Wetherall	5th Edition	Pearson Education
2	Software Defined Networks – A Comprehensive Approach	Paul Goransson, Chuck Black and Timothy Culver	2nd Edition, 2017	Morgan Kaufmann
Reference Books:				
1.	Data Communications and Networking	Behrouz A. Forouzan	Fourth Edition,2007	Tata McGraw Hill
2.	Computer Networking- A Top down Approach Featuring the Internet	James F Kurose, Keith W Ross	7th Edition, 2017	Pearson Education

Web links and Video Lectures (e-resources)
https://onlinecourses.nptel.ac.in>noc23_cs35
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study

5. Learn by Doing

PART-B		
Academic year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED COMPUTER NETWORKING**		
Course Code: **P24MECE142**	CIE marks: 50	CIE Weightage:50%
Teaching hours/weeks (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy 40 hrs	Exam hours: 3	
Credits**: 03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Understand advanced concepts and next generation networks.	L1	PO1,PO2,PO4
CO2: Analyze network Algorithm's, Protocols and their functionalities.	L2	PO1,PO2,PO3,PO4,PO5
CO3: Comprehend features of SDN and its application to next generation systems	L3	PO1,PO2,PO3,PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3	2		2		3	2
CO2	3	3	2	3	2	3	3
CO3	2	2	2		2	2	2

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED SIGNAL PROCESSING**		
Course Code**: P24MECE143**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hrs	
Credits:**03**		
Prerequisite:		
Signals & Systems, Digital Signal Processing.		
Course learning Objectives:		
CLO1: Explore & understand algorithms & techniques of Signal processing in context real time applications. CLO2: Learn analysing discrete time signals &systems. CLO3: Design Sub-blocks of signal processing systems. CLO4: Apply the knowledge of signals & algorithms in developing signal processing blocks.		
UNIT -1		8 Hours
Analysis of Discrete Time Signals: Basic elements of a DSP System –Review of Sampling and Quantisation – Sampling theorem for low pass and band pass signals, uniform and non-uniform quantization, Application of quantisation in lossy compression of signals – Lloyd Max quantizer; Fourier analysis of Continuous and Discrete time signals – Review of Fourier series and Fourier transform, Discrete Time Fourier Transform(DTFT),Discrete Fourier Transform (DFT), Interpretation of DFT Spectrum, Review of DFT properties –Convolution and correlation, Convolution of long sequences, Leakage effect, Windowing – Introduction to other transforms : Discrete Cosine Transform (DCT), Walsh Hadamard Transform (WHT), Karhunen Loeve Transform (KLT) – Applications. **RBTLevels:**L2,L3		
Self-Study Content: Walsh Hadamard Transform (WHT)– Applications		
Textbook Map: Text 1-2.1-2.13,3.1-3.7		
Teaching Learning Process: power point presentation with demonstration(MATLAB Simulation)		
UNIT 2:		8 Hours
Digital Filters and Implementation: Review of FIR and IIR filter design – Notch filter– Comb filter– All pass filters – Applications – Structures for digital filter realization: Signal flow graph and block diagram representations, FIR and IIR Filter structures, Lattice structures – Finite word length effects – Fixed-point and floating-point DSP arithmetic, Effects of quantization, Scaling, Limit cycles in fixed point realizations of IIR digital filters, Limit cycles due to overflow. Quantization effect in DFT and FFT computation. **RBTLevels:**L3,L4		
Self-Study Content: Quantization effect in DFT and FFT – Applications		
Textbook Map: Text 1-4.1-4.11.		
Teaching Learning Process: power point presentation with Case Studies.		
UNIT 3:		8 Hours
Multirate Signals and Systems: Introduction to multirate signal processing with applications, Multirate System Fundamentals – Decimation and Interpolation, Transform domain analysis of Decimators and Interpolators, Decimation and Interpolation filters, Fractional sampling rate alteration, Practical sampling rate converter design. **RBTLevels:**L3,L4		

Self-Study Content: Decimation and Interpolation – Applications	
Textbook Map: Text 2-2.1-2.8,3.1-3.7	
Teaching Learning Process: power point presentation with guest lecturer.	
UNIT 4:	8 Hours
Introductionto2-DSignalsandSystems: Polyphase decomposition and efficient structures – Introduction to digital filter banks – The DFT filter bank, Two Channel Quadrature Mirror Filter bank (QMF), Perfect Reconstruction.	
Self-Study Content: DFT filter bank – Applications	
Textbook Map: Text 3-1.1-1.8.	
Teaching Learning Process: power point presentation with examples.	
UNIT 5:	8 Hours
Introduction to2-D Signals and Systems: Elementary 2D signals–Linear shift Invariant systems–Separability – 2Dconvolution–Introductionto2Dtransforms:2DDFT,2DDCT, Applications. **RBTLevels:**L3,L4	
Self-Study Content: 2Dconvolution– Applications	
Teaching Learning Process: power point presentation with examples.	
Textbook Map: Text 3-2.1-2.8,3.1-3.3	
Course Outcomes: At the end of the course students should be able to :	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Digital Signal Processing: Principles, Algorithms and Applications,	John G. Proakis, Dimitris G. Manolakis	2007, 4thEdition	Pearson India
2	Multirate systems and filter banks	P.P.Vaidyanathan	1992, 2ndEdition	Pearson Education India
	Two dimensional signal and image processing	LimJ.S	1990.	Prentice Hall
Reference Books:				
1.	Digital Signal Processing: Theory and Practice	K Deergha Rao,MNS Swamy	2018.	Springer
2.	The Scientist and Engineer's Guide to Digital Signal Processing	StevenW.Smith	1999	California
3.	Digital Signal Processing: A Computer Based Approach	MitraS.K	2013	McGraw-Hill Publishing Company

Web links and Video Lectures (e-resources)
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study

5. Learn by Doing

PART-B		
Academic year:2024-25	**Semester:**I	**Scheme:**P24
Course Title: : **ADVANCED SIGNAL PROCESSING**		
Course Code: P24MECE143	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hrs	
Credits:03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Analyze the effect of sampling and quantisation of signals and appraise its relevance with reference to applications.	L2	PO1
CO2: Formulate various transform domain representationsof1Dand2Dsignalsand demonstrate their applications with reference to practical signals.	L4	PO1
CO3: Examine finite word length effects in real time signal processing.	L2	PO3
CO4: Illustrate the effect of sampling rate converters and design distortion free digital filter banks illustrating their applications to process real life signals.	L2	PO3
CO5: Identification & design of DSP architectures for given requirements.	L5	PO2

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2	2					2	
CO3			1				
CO4			1				
CO5		2					2

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **POWER CONVERTERS**		
Course Code: **P24MECE144**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	
Credits:**03**		
Prerequisite:		
Basic Electronics, Analog Electronics Circuits, Power Electronics		
Course learning Objectives:		
CLO1: To analyze Power diodes and rectifiers. CLO2: To analyze and design DC to DC converters. CLO3: To analyze DC to AC converters. CLO4: To analyze Switched circuits. CLO5: To analyze AC Voltage Regulators.		
UNIT -1		8 Hours
Power Diodes and Rectifiers: Introduction, Performance Parameters, Single-Phase Full-Wave Rectifiers, Single-Phase Full-Wave Rectifier with *RL* Load, Single-Phase Full-Wave Rectifier with a Highly Inductive Load, Three-Phase Bridge Rectifiers, Three-Phase Bridge Rectifier with *RL* Load, Three-Phase Rectifier with a Highly Inductive Load, Comparisons of Diode Rectifiers, Rectifier Circuit Design, Output Voltage with *LC* Filter.		
Self-Study Content:1. Effects of Source and Load Inductances. 2. Practical Considerations for Selecting Inductors and Capacitors		
Textbook1:3.1-3.5, 3.7-3.12		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
Analysis and design of DC to DC converters: Introduction, Performance Parameters of DC–DC Converters, Principle of Step-Down Operation, Step-Down Converter with *RL* Load, Principle of Step-Up Operation, Step-Up Converter with a Resistive Load, Frequency Limiting Parameters, Converter Classification, Switching-Mode Regulators, Comparison of Regulators.		
Self-Study Content: 1. Multi output Boost Converter, 2. Diode Rectifier-Fed Boost Converter, 3. Design Considerations for Input Filter and Converters		
Textbook1: 5.1 – 5.10		
Teaching Learning Process: PPT		
UNIT 3:		8 Hours
Analysis and design of DC to AC converters: Introduction, Performance Parameters, Principle of Operation, Single-Phase Bridge Inverters, Three-Phase Inverters, Voltage Control of Single-Phase Inverters, Harmonic Reductions, Current-Source Inverters.		
Self-Study Content:1. Boost Inverter 2. Inverter Circuit Design		
Textbook1: 6.1-6.6, 6.8, 6.9		
Teaching Learning Process: PPT		
UNIT 4:		8 Hours
Analysis of switched circuits: **Thyristor:** Introduction, Thyristor Characteristics, Two-Transistor Model of Thyristor. **Controlled Rectifiers:** Introduction, Single-Phase Full Converters, Single-Phase Dual		

Converters, Three-Phase Dual Converters, Single-Phase Series Converters.

Self-Study Content:1. Thyristor Types
2. Twelve-Pulse Converters
3. Design of Converter Circuits

Textbook1: 9.1-9.3, 10.1,10.2,10.3,10.4,10.7

Teaching Learning Process: Case Study

UNIT 5:	8 Hours

AC Voltage Regulators: Introduction, Performance Parameters of AC Voltage Controllers, Single-Phase Full-Wave Controllers with Resistive Loads, Single-Phase Full-Wave Controllers with Inductive Loads, Three-Phase Full-Wave Controllers, Three-Phase Full-Wave Delta-Connected Controllers, Single-Phase Transformer Connection Changers, Cyclo converters, AC Voltage Controllers with PWM Control, Matrix Converter.

Self-Study Content: 1. Design of AC Voltage-Controller Circuits
2. Effects of Source and Load Inductances

Teaching Learning Process: Case Study

Textbook1: 11.1-11.10

Course Outcomes: At the end of the course students should be able to :

CO1: Analyse the Power diodes and rectifiers.
CO2:Analyze and Design DC to DC converters.
CO3: Analyze and Design the DC to AC converters.
CO4:Analyze the Switched circuits
CO5:Analyze the AC Voltage Regulators

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1.	Power Electronics Devices, Circuits, and Applications	Muhammad H. Rashid	2014. Fourth Edition	Pearson Education Limited

Reference Books:

1.	PowerElectronics:converters,Applicationanddesign’	NedMohan,UndelandandRobbin	2003. Third Edition	JohnWiley
2.	Principles of Electric Machines and PowerElectronics	P.CSen.,	2007 Second Edition,NewDelhi,	JohnWiley

Web links and Video Lectures (e-resources)

1.https://pdfcoffee.com/power-electronics-converters-applications-and-design-third-edition-ned-mowpdf-pdf-free.html
2.https://archive.nptel.ac.in/courses/117/103/117103148/
3.https://archive.nptel.ac.in/courses/108/102/108102157/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	**Semester:**I	**Scheme:**P24
Course Title: **POWER CONVERTERS**		
Course Code: **P24MECE144**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	
Credits:03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Analyse the Power diodes and rectifiers.	L2	PO2,PO5
CO2: Analyze and Design DC to DC converters.	L2, L3	PO2, PO5
CO3: Analyze and Design the DC to AC converters.	L2,L3	PO2, PO4
CO4: Analyze the Switched circuits	L2	PO2, PO3
CO5: Analyze the AC Voltage Regulators	L2	PO2, PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1		2			2		2
CO2		2			2		2
CO3		2		2			2
CO4		2	2				2
CO5		2		2			2

PROFESSIONAL ELECTIVE 2		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED EMBEDDED SYSTEMS**		
Course Code: **P24MECE151**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Prerequisite:		
Basic knowledge of digital electronics, Embedded systems concepts, including microcontroller programming and familiarity with C/C++ programming languages.		
Course learning Objectives:		
CLO1: To understand the difference between Embedded Systems and General Computing Systems. CLO2: To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems CLO3: Analysis of a Real Life example on the bonding of Embedded Technology with Human Life CLO4: To understand the difference between Microcontrollers and ARM Cortex processors. CLO5: To learn Programming using assembly and C language, CMSIS for variety of End Applications.		
UNIT -1		8 Hours
Embedded System: Embedded v/s General Computing System, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opt coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.		
Self-Study Content:1. Explore how Embedded systems perform specific tasks in automotive, medical, and electronics. 2. Study UART, I2C, SPI protocols and SOC design tools.		
Textbook Map:-Text 1: 1.1-1.6,2.1-2.7,3.1-3.2		
Teaching Learning Process: Flipped Classroom/PPT		
UNIT 2:		8 Hours
Hardware Software Co-Design: Embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging.		
Self-Study Content: 1. Learn C, C++, and assembly languages for embedded system development. 2. Discuss the tools are available for the Embedded system design		
Textbook Map: Text 1: 9.1-9.2,12.1,13.1-13.4		
Teaching Learning Process: Quiz/PPT		
UNIT 3:		8 Hours
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM CortexM3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.		
Self-Study Content: 1. Compare ARM 32-bit architecture with other microcontroller architectures. 2. Prepare the report on in today electronics industry.		

Textbook Map: Text 2:1.1-1.5,2.1-2.9,3.1-3.7	
Teaching Learning Process: Think Pair share- peer teaching/PPT	
UNIT 4:	8 Hours
InstructionSets: Assemblybasics,Instructionlistanddescription,usefulinstructions,MemorySystems,Memorymaps,CortexM3implementationoverview,pipelineandbusinterface,Exceptions,NestedVectorinterruptcontrollerdesign,SystickTimer,Cortex-M3ProgrammingusingassemblyandClanguage,CMSIS.	
Self-Study Content:1. Identify the usage of Memory Systems in real time. 2. Explore programming ARM Cortex-M3 microcontrollers using both assembly and C language.	
Textbook Map: Text 2:4.1-4.4,5.1-5.8,6.1-6.7,7.1-7.6,8.1-8.5,10.1-10.8	
Teaching Learning Process: Seminar/ PPT	
UNIT 5:	8 Hours
Introduction to RISC-V: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization	
Self-Study Content:1. Study how operands are used and processed in RISC-V hardware. 2. Explore how instructions are represented and stored in RISC-V systems.	
Textbook Map: Text 3: 2.1-2.11	
Teaching Learning Process: Seminar/PPT	
Course Outcomes: At the end of the course students should be able to :	
CO1: **Understand** and apply knowledge of electronic circuits to explore the features of the ARM Cortex-M3, and design a real-time system that leverages its processing power, efficient interrupt handling, and power efficiency for performance. CO2: **Demonstrate** the use of a specific firmware design approach in the code design process. CO3: **Develop** the code for ARM Cortex-M3 microcontrollers using both assembly and C language. CO4: **Design** and implement an advanced embedded system that integrates RISC-V processor features using any suitable tool.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Introduction to embedded systems	K.V.Shibu	2009	TMH education Pvt. Ltd
2	The Definitive Guide to the ARM Cortex-M3	Joseph Yiu, Newnes,(Elsevier)	2010	2nd Edition
3	Computer Organization and Design RISC-V Edition	David A.Patterson, John L.Hennessy, Morgan Kaufmann	2018	ISBN: 9780128122761.

Reference Books:				
1.	Embedded systems-A	James K.Peckol,	2008	2nd Edition

	contemporary design tool	John Wiley		

Web links and Video Lectures (e-resources)

1. https://nptel.ac.in/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **ADVANCED EMBEDDED SYSTEMS**		
Course Code: **P24MECE151**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam hours:3 Hours	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Understand and apply knowledge of electronic circuits to explore the features of the ARM Cortex-M3, and design a real-time system that leverages its processing power, efficient interrupt handling, and power efficiency for performance.	.L1	PO1
CO2: Demonstrate the use of a specific firmware design approach in the code design process.	L2	PO2
CO3: Develop the code for ARM Cortex-M3 microcontrollers using both assembly and C language.	L5	PO3
CO4: Design and implement an advanced embedded system that integrates RISC-V processor features using any suitable tool	L5	PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3			2				
CO4				3			

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED WIRELESS COMMUNICATION**		

Course Code: **P24MECE152**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P)= 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Prerequisite:		
Fundamentals of digital communication signal processing, and wireless network.		
Course learning Objectives:		
CLO1: To enable students understand the various aspects of wireless communication CLO2: To understand the concept behind the capacity of channels CLO3: Gain the information on Linear time-invariant Gaussian channels, Capacity off adding channels CLO4: Study uplink and downlink model of AWGN channel, fading channels CLO5: Describe different types of diversity, Understanding concept behind modelling of MIMO		
UNIT -1		8 Hours
Physical modelling for wireless channels, Input/output model of the wireless channel: Free space, Fixed transmit and receive antennas, Free space, moving antenna, Reflecting wall, fixed antenna, Reflecting wall, moving antenna Reflection from a ground plane, Power decay with distance and shadowing, Moving antenna, multiple reflectors, The wireless channel as a linear time-varying system, Baseband equivalent model, discrete time baseband model, Additive white noise		
Self-Study Content: **1**.Understand the input/output channel relationship, including channel impulse response, Doppler effect, and noise impacts.		
Textbook Map: **2.1 to 2.2**		
Teaching Learning Process: Quiz/Seminar/Case Study/PPT		
UNIT 2:		8 Hours
Time and frequency coherence, AWGN channel capacity: Time and frequency coherence: Doppler spread and coherence time, delay spread and coherence bandwidth, Repetition coding, Packing spheres, Capacity-achieving AWGN channel codes, Reliable rate of communication and capacity, Resources of the AWGN channel-Continuous-time AWGN channel, Power and bandwidth, Bandwidth reuse in cellular systems.		
Self-Study Content: **1**.Understand how channel stability impacts signal transmission over time and frequency. **2**. Learn AWGN channel capacity using Shannon's theorem, focusing on the relationship between bandwidth, SNR, and maximum data rate.		
Textbook Map: **2.3, 5.1 to 5.2**		
Teaching Learning Process: Quiz/Seminar/Case Study/PPT		
UNIT 3:		8 Hours
Linear time – invariant Gaussian channels, Capacity of adding channels : Single input multiple output(SIMO) channel, Multiple input single output(MISO) channel, Frequency-selective channel, Slow fading channel, receive diversity, Transmit diversity, Transmit and receive diversity, Time and frequency diversity, Outage for parallel channels, Fast fading channel, Transmitter side information, Frequency-selective fading channels		
Self-Study Content: **1**. Explore linear time-invariant (LTI) Gaussian channels, focusing on how they model stable channels with constant properties over time.		
Textbook Map: **5.3 to 5.4**		
Teaching Learning Process: Quiz/Seminar/Case Study/PPT		
UNIT 4:		8 Hours
Uplink and Downlink AWGN channel, Uplink and Downlink fading channel: Capacity via Successive interference cancellation, Comparison with conventional CDMA, Comparison		

with orthogonal multiple access, General K-user uplink capacity, Symmetric case: Two capacity achieving schemes, General case: super position coding achieves capacity, Slow fading channel, Fast fading channel, Full channel side information, Channel side information at receiver only, Full channel side information, Frequency selective fading channels.

Self-Study Content: **1**.What role does power control play in managing uplink and downlink performance in fading environments.

Textbook Map: **6.1 to 6.5**

Teaching Learning Process: Quiz/Seminar/Case Study/PPT

UNIT 5: 8 Hours

Multi user diversity, Physical Modeling of MIMO channels: Multiuser diversity gain, Multiuser versus classical diversity, Fair scheduling and multi user diversity, Channel prediction and feedback, Opportunistic beam forming using dumb antennas ,Multiuser diversity in multi cell systems, Line-of-sight SIMO channel, Line-of-sight MISO channel, Antenna arrays with only a line-of- sight path, Geographically separated antennas, Line-of-sight plus one reflected path, MIMO multipath channel, Angular domain representation of signals, Angular domain representation of MIMO channels, Statistical modeling in the angular domain, Degrees of freedom and diversity, Dependency on antenna spacing.

Self-Study Content: **1**.Explore physical modeling of MIMO channels to learn how spatial multiplexing and diversity enhance capacity and reliability in wireless systems.

Teaching Learning Process: Quiz/Seminar/Case Study/PPT

Textbook Map: **6.6 to 6.7, 7.2 to 7.3**

Course Outcomes: At the end of the course students should be able to :

CO1: Apply knowledge of communication systems to understand physical wireless channel models.
CO2: Examine the effects of key parameters on the capacity of AWGN, LTI Gaussian, and fading channels.
CO3: Develop advanced techniques to accurately model and estimate multiuser channels for effective resource allocation.
CO4: Simulating the performance of various uplink and downlink models using existing tools.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Fundamentals of Wireless Communications	David Tse, Pramod Viswanath		Cambridge University Press, 2005 ISBN: 978-0-521-84527-4
2	Wireless Communications	Andrea Goldsmith	2nd Edition	Cambridge University Press,2005 ISBN-10 : 9780521704168 ISBN-13 : 978-0521704168

Reference Books:

1.	Wireless Communications: Principles and Practice	Theodore Rappaport.	2nd Edition	Pearson Education India ISBN 9332576165, 9789332576162
2.	Wireless Communication Systems	Ke-Lin Du and M. N. S. Swamy		Cambridge University Press, 2010 ISBN: 0521114039,9780521114035

Web links and Video Lectures (e-resources)				
.https://nptel.ac.in/				
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)				
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing				

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title**: ADVANCED WIRELESS COMMUNICATION**		
Course Code: **P24MECE152**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P)= 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Apply knowledge of communication systems to understand physical wireless channel models	L3	PO1
CO2: Examine the effects of key parameters on the capacity of AWGN, LTI Gaussian, and fading channels	L3	PO3
CO3: Develop advanced techniques to accurately model and estimate multiuser channels for effective resource allocation.	L4	PO3
CO4: Simulating the performance of various uplink and downlink models using existing tools.	L5	PO2,PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2			2				
CO3		1					1
CO4		1	1				1

PART-B		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **MULTIMEDIA AND APPLICATIONS**		
Course Code: **P24MECE153**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P)=3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3(Theory)	

Credits: **03**	
Prerequisite:	
Basic knowledge of multimedia including text, image, audio, video including network terminology. Additionally an understanding of different multimedia compression techniques is recommended.	
Course learning Objectives:	
CLO1:Understand different multimedia encoding schemes and principles of compression algorithms CLO2:Apply the encoding techniques for given data. CLO3:Understand the mechanism of audio and video compression techniques and multimedia networks.	
UNIT -1	8 Hours
Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video. **RBT Levels:** L2	
Self-Study Content: Prepare a report of historical representation of multimedia information representation.	
Textbook Map:1.1, 1.2,1.3,1.4,1.5, Ch 2:2.2-2.6	
Teaching Learning Process: Power point presentation with case studies	
UNIT 2:	8 Hours
Text and image compression: Compression principles, Text compression-Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression-GIF, TIFF and JPEG. **RBT Levels:** L3	
Self-Study Content: Understand the decoding of received bit stream.	
Textbook Map: 3.1, 3.2,3.3.5,3.4.1,3.4.2,3.4.5	
Teaching Learning Process: Power point presentation with case studies	
UNIT 3:	8 Hours
Audio and Video Compression: Audio compression– principles, DPCM, ADPCM Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles. **RBT Levels:** L3	
Self-Study Content: Error resilience techniques	
Textbook Map:4.1,4.2,4.3, 4.3.1	
Teaching Learning Process: Power point presentation with seminars	
UNIT 4:	8 Hours
Video Compression Standards:H.261, H.263, MPEG, MPEG1, MPEG2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework. **RBT Levels:**L3	
Self-Study Content: Basics of computer based animation	
Textbook Map:4.3.2,4.3.3,4.3.4,4.3.5,4.3.6 ,4.3.7,4.3.4, 3.6	
Teaching Learning Process:Powerpoint presentation with guest lecture	
UNIT 5:	8 Hours
Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD). **RBT Levels:** L3, L4	
Self-Study Content: Understand general concepts of token rings and FDDI.	

Teaching Learning Process: Power point presentation with group discussion

Textbook Map:9.1,10.4.2,1.4.3

Course Outcomes: At the end of the course students should be able to :

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Multimedia Communications: Applications, Networks, Protocols and Standards	Fred Halsall,Pearson Education Publishers	2001	ISBN: 97802013981871.
2	Multimedia: Computing, Communications andApplications	Raif Steinmetz, KlaraNahrstedt	2002	

Reference Books:

1.	Multimedia Communication Systems	K.R.Rao,Zoran S.Bojkovic, DragoradA.Milovanovicm	2004	
2.	Multimedia Networks: Protocols, Design and Applications	Hans. W. Barz, Gregory A. Bassett	2016	ISBN:9781119090137
3.	Multimedia: An Introduction	John Billamil, Louis Molina	2002	

Web links and Video Lectures (e-resources)

1.https://nptel.ac.in/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **MULTIMEDIA AND APPLICATIONS**		
Course Code: **P24MECE153**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P)=3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3(Theory)	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Compare encoding schemes, multimedia techniques and multimedia communication models.	L2	PO2
CO2: Illustrate the working of encoding schemes and multimedia algorithms.	L2	PO2
CO3: Design a subsystem and/or multimedia framework for given requirements.	L4	PO2
CO4: Analyse the impact and effectiveness of multimedia technique, routing technique and multimedia network.	L3	PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1		2					2
CO2		2					2
CO3		2					2
CO4					2		

PART-B		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **PROCESS CONTROL**		
Course Code: **P24MECE154**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
Electronic and Instrumentation, Control System		
Course learning Objectives:		
CLO1: To understand the need of process control, basic principles of various manufacturing processes. CLO2: Apply engineering knowledge to do problem analysis in process control. CLO3: To select the proper controller and apply the tuning rules to achieve optimum performance. CLO4:To understand and interpret the predictive Control, Multivariate Statistical Techniques CLO5: Apply knowledge of process control in Bio systems control design.		
UNIT -1		8 Hours
Introduction to Process Control- Representative Process Control Problems, Illustrative Example—A Blending Process, Classification of Process Control Strategies, A More Complicated Example—A Distillation Column, The Hierarchy of Process Control Activities, An Overview of Control System Design. **Theoretical Models of Chemical Processes-**The Rationale for Dynamic Process Models, General Modeling Principles, Degrees of Freedom Analysis, Dynamic Models of Representative Processes, Process Dynamics and Mathematical Models		
Self-Study Content: Laplace Transforms of Representative Functions, Solution of Differential Equations by Laplace Transform Techniques, Partial Fraction Expansion		
Textbook Map: 1.1– 1.6, 2.1– 2.5		
Teaching Learning Process: Poster presentation/Quiz/Seminar/Team demonstration		
UNIT 2:		8 Hours
Transfer Function Models- Introduction to Transfer Function Models, Properties of Transfer Functions, Linearization of Nonlinear Models **Dynamic Behaviour of First-Order and Second-Order Processes-** Standard Process Inputs, Response of First-Order Processes, Response of Integrating Processes, Response of Second-Order Processes		
Self-Study Content: Dynamic Behaviour and Stability of Closed-Loop Control Systems, Closed-Loop Transfer Functions, Closed-Loop Responses of Simple Control Systems.		
Textbook Map: 4.1- 4.3, 5.1- 5.4		
Teaching Learning Process: Flip class/Quiz/Seminar/Team demonstration		
UNIT 3:		8 Hours
Dynamic Response Characteristics of More Complicated Processes- Poles and Zeros and Their Effect on Process Response, Processes with Time Delays, Approximation of Higher-Order Transfer Functions, Interacting and Non interacting Processes, State-Space and Transfer Function Matrix Models, Multiple-Input, Multiple-Output (MIMO) Processes. **Development of Empirical Models from Process Data-** Model Development Using Linear or Nonlinear Regression, Fitting First- and Second-Order Models Using Step Tests, Neural Network Models, Development of Discrete-Time Dynamic Models**,** Identifying Discrete-Time Models from Experimental Data.		
Self-Study Content: Performance Criteria for Closed-Loop Systems, Model-Based Design		

Methods, Controller Tuning Relations, Controllers with Two Degrees of Freedom.	
Textbook Map: 6.1- 6.6, 7.1- 7.5	
Teaching Learning Process: Quiz/Seminar/Team demonstration/One minute paper writing	
UNIT 4:	8 Hours
Feedback Controllers- Introduction**,** Basic Control Modes, Features of PID Controllers, Digital Versions of PID Controllers, Typical Responses of Feedback Control Systems, On–Off Controllers. **Control System Instrumentation-** Sensors, Transmitters, and Transducers, Final Control Elements Accuracy in Instrumentation	
Self-Study Content: Process Safety and Process Control, Layers of Protection, Alarm Management, Abnormal Event Detection, Risk Assessment	
Textbook Map: 8.1- 8.6. 9.1- 9.3	
Teaching Learning Process: Think pair share/One minute paper writing/ Quiz/Seminar	
UNIT 5:	8 Hours
Model Predictive Control - Overview of Model Predictive Control, Predictions for SISO Models**,** Predictions for MIMO Models **Process Monitoring-**Traditional Monitoring Techniques, Quality Control Charts, Multivariate Statistical Techniques **Bio systems Control Design-** Process Modelling and Control in Pharmaceutical Operations, Process Modelling and Control for Drug Delivery	
Self-Study Content: Model Predictive Control Calculations, Set-Point Calculations, Selection of Design and Tuning Parameters, Control Performance Monitoring	
Teaching Learning Process: One minute paper writing/ Quiz/Seminar/Team demonstration	
Textbook Map: 20.1, 20.2, 20.3, 21.1, 21.2, 21.4, 23.1, 23.2.	
Course Outcomes: At the end of the course students should be able to :	

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	"Process Dynamics and Control"	D. E. Seborg, T.F. Edgar, D. A. Mellichamp	2004, Fourth Edition	Wiley
2	"Chemical Process Control An Introduction to Theory and Practice"	G. Stephanopolous	August 2000.	Prentice Hall India,

Reference Books:

1.	"Process Control Instrumentation Technology"	C.D. Johnson,	2014	Prentice Hall India.
2.	"Process Control Systems Application Design and Adjustment"	F.G. Shinskey	3rd edition,	McGraw Hill International, 6. D.

Web links and Video Lectures (e-resources)

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation

3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **PROCESS CONTROL**		
Course Code: **P24MECE154**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Apply knowledge to implement process control systems using theoretical and mathematical models.	**L3**	**PO1**
CO2: Analyze empirical models from process data to predict chemical process dynamics and design control strategies.	**L4**	**PO2**
CO3: Design and implement feedback controllers, select instrumentation, and tune parameters for optimal performance.	**L6**	**PO1**
CO4: Develop process control systems with sensors, actuators, and optimization for efficient operation.	**L6**	**PO4**

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2		2					2
CO3	2					2	
CO4				2			

VLSI DESIGN LAB			
Course Code	**P24MECEL16**	CIE Marks	50
Teaching Hours/Week(L:P:T/SDA)	0:1:1	SEE Marks	50

Credits	02	Exam Hours	03(Practical)

Course Objectives:

- To Familiarize with the ASIC flow and cadence tool suite
- To Debug and develop RTL code
- To perform functional verification, Logical equivalence check(LEC), Timing and power analysis.
- To Develop embedded code for the given requirements
- To perform testing and verification of multithread application.

Sl.No.	Experiments
	Part–A **VLSI Digital Design**
1	Write Verilog Code for the following circuits and their Test Bench for verification, ➢ An inverter, Buffer and Transmission gate ➢ Basic/Universal gates ➢ Flip flop -RS, D, JK, MS, T
2	Write Verilog code for the following circuits and their Test Bench for verification ➢ Carry Ripple Adder ➢ Carry Look Ahead adder ➢ Carry Skip Adder
3	Design the following circuits using ASIC Digital Design flow and Write a Verilog Code for 8-bit Booth Multiplication (Radix-4)
4	Design the following circuits using ASIC Digital Design flow and Write Verilog code for 4/8-bit Magnitude Comparator, Parity Generator,
5	Design the following circuits using ASIC Digital Design flow and Write Verilog code for 4/8-bit, LFSR, Universal Shift Register
6	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
	Part–B **VLSI Analog Design (Upto Post Layout Simulation)**
7	Design single stage differential amplifier
8	Design a simple 4/8-bit ADC converter
9	Design an op-amp with given specification* using differential amplifier Common source amplifier in library**

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. **Develop** RTL code/Embedded code for given requirement
2. **Analyze** the given RTL/Embedded code.
3. **Debug** the given RTL/Embedded code
4. **Design** and **simulate** a module/system for given requirements

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is 50 Marks.

The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The test marks is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours

Suggested Learning Resources:

- **"Introduction to Embedded Systems",** Shibu K V, TMH Education Pvt Ltd, Second reprint, 2010, ISBN(13): 978-0-07-014589-4.
- **"Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology: Circuit Design, and Process Technology"** Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, CRC Press, ISBN-10: 0-8493-7924-5, ISBN-13: 978-0-8493-7924-6, 2006**..**
- **"Digital VLSI Design (RTL to GDS)"**Dr. Adam Teman , Emerging nano scaled Integrated Circuits and Systems (En ICS) Labs Faculty of Engineering, Bar-Ilan University

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	

CO2		2					2
CO3	2					2	
CO4			3				

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Design of Analog and Mixed Mode VLSI Circuits**		
Course Code: **P24MECE21**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:2	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **04**		
Prerequisite:		
Prerequisite: 1. Basics of electronics 2. Circuit analysis 3. Signals and converters		
Course learning Objectives:		
CLO1: To understand the basic physics and operation of MOS devices. CLO2: To study, analyse and design Single-Stage and Differential Amplifiers. CLO3: To analyse the amplifiers for different characteristics and responses. CLO4: To Design Oscillators of given specifications. CLO5: To Understand architecture of Data converter includes ADC (Analog to Digital) and DAC (Digital to Analog) Converters.		
UNIT -1		8 Hours
Basic MOS Device Physics: General considerations, MOS1/V Characteristics, second order effects, MOS device Models. **Single stage Amplifier**: Basic Concepts, Common Source stage, Source follower.		
Self-Study Content: Basic Current Mirrors, Cascade Current Mirrors.		
Text book Map: **2.1 to 2.4, 3.1 to 3.4 (Text 1)**		
Teaching Learning Process: PPT/chalk and talk, Seminar.		
UNIT 2:		8 Hours
Single stage Amplifier: Common-gate stage, Cascade Stage. **Differential Amplifiers**: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.		
Self-Study Content: Feedback Topologies (Voltage – Voltage Feedback, Current – Voltage, Voltage – Current, Current – Current Feedback).		
Text book Map**: 3.1 to 3.6, 4.1 to 4.5 (Text 1)**		
Teaching Learning Process: PPT/chalk and talk/simulation.		
UNIT 3:		8 Hours
Frequency Response of Amplifiers: General Considerations , Miller Effect, Association of Poles with Nodes, Common-Source Stage ,Source Followers. **Noise**: Statistical Characteristics of Noise, Noise Spectrum, Amplitude Distribution, Correlated and Uncorrelated Source, Signal-to-Noise Ratio, Noise Analysis Procedure, Types of Noise, Thermal Noise, Flicker Noise, Representation of Noise in Circuits, Noise in Single-Stage Amplifiers, Common-Source Stage, Common-Gate Stage.		
Self-Study Content: Multipole Systems, Phase Margin.		
Text book Map: **6.1 to 6.3, 7.1 to 7.4.2 (Text 1)**		
Teaching Learning Process: PPT/chalk and talk /Individual Role play/Team Demonstration.		
UNIT 4:		8 Hours
Oscillators: General Considerations, Ring Oscillators, LC Oscillators, Basic Concepts, Cross-Coupled Oscillator, Colpitts Oscillator. **Phase-Locked Loops**: Simple PLL, Phase Detector, Basic PLL Topology, Dynamics of Simple PLL.		
Self-Study Content: PFD/CP Non idealities, Jitter in PLLs.		
Text book Map: **15.1 to 15.3.3, 16.1 to 16.1.3 (Text 1).**		

Teaching Learning Process: PPT/chalk and talk / Individual Role play/Team Demonstration.

UNIT 5:	8 Hours

Data Converter Architectures : DAC & ADC Specifications, Digital Input Code, Resistor Steering, R-2R Ladder Networks, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Successive Approximation ADC.

Self-Study Content: Mixed Mode Layout Issues.

Text book Map: **29.1 to 29.1.7, 29.2, 29.2.1, 29.2.5 (Text 2)**

Teaching Learning Process: PPT/chalk and talk/Flip class/ Case study.

Course Outcomes: At the end of the course students should be able to :

CO1: Analyse amplifiers, oscillators and data converter circuits.
CO2: Design amplifiers, oscillators and data converters for given specifications.
CO3: Simulate and analyse the characteristics of the given analog or mixed mode circuit.
CO4: Write a technical report on the given design/research article.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Design of Analog CMOS Integrated Circuits, 2nd Edition.	Behzad Razavi	2007	ISBN 978-0-07-252493-2 MHID 0-07-252493-6
2	CMOS Circuit Design, Layout and Simulation, Wiley Second Edition	R.Jacob Baker	1988	ISBN 0-07-029158 - 6

Reference Books:

1.	CMOS Analog Circuit Design, Second Edition, Oxford University Press.	Phillip E. Allen, Douglas R. Holberg,	2002	ISBN 0-19-511644 – 5 Oxford University Press

Web links and Video Lectures (e-resources)

1. VTU e-learning Resources

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **Design of Analog and Mixed Mode VLSI Circuits**		
Course Code: **P24MECE21**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:2	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Analyse amplifiers, oscillators and data converter circuits and responses.	L4	PO1
CO2: Design amplifiers, oscillators and data converters for given specifications.	L3	PO1
CO3: Simulate and analyse the characteristics of the given analog or mixed mode circuits and present a summary of the same.	L4	PO3
CO4: Write a technical report on the given design/research article/scenario.	L5	PO2,PO6

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2	3					3	
CO3			3				
CO4		1			1		

Practical Component of IPCC

Sl.No	Experiments
1	Design an op-amp with given specification* using differential amplifier Common source amplifier in library. (Applicable Library should be added & information should be given to the Designer.)
2	Designa 4 bit R-2R based DAC for the given specification (Applicable Library should be added & information should be given to the Designer.)
3	Design an Integrator using OPAMP (First Order)
4	Design a Differentiator using OPAMP (First Order)
5	Design and characterize a basic Sigma delta ADC from the available designs.

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **VLSI Testing and Verification**		
Course Code: **P24MECE22**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
1. Fundamental of digital electronics 2. HDL programming		
Course learning Objectives:		
CLO1: To study Faults in digital circuits. CLO2: To learn various algorithms for test generation of Combinational Logic Circuits. CLO3: To study the approach to deal with the testing problems at the chip level (BIST). CLO4: To know about Design Verification Concepts, Simulator Architectures and Operations.		
UNIT -1		8 Hours
Faults in digital circuits: Failures and Faults, Modelling of faults, Temporary Faults. **Test generation for Combinational Logic circuits:** Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits (One Dimensional Path Sensitization, Boolean Difference, D-Algorithm).		
Self-Study Content: The Reed-Muller Expansion Technique, Three-Level OR-AND-OR Design		
Text book Map: Text 1: 1.1-1.3, 2.1, 2.2.1, 2.2.2, 2.2.3		
Teaching Learning Process: Flipped Classroom		
UNIT 2:		8 Hours
Test generation for Combinational Logic circuits: Test generation techniques for combinational circuits (PODEM, FAN, Delay Fault Detection), Detection of multiple faults in Combinational logic circuits. **Design of test able sequential circuits:** Controllability and Observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, The scan-path technique for testable sequential circuit design.		
Self-Study Content: Testing of Sequential Circuits as Iterative Combinational Circuits		
Text book Map: Text 1: 2.2.4, 2.2.5,2.2.6, 2.3, 5.1,5.2,5.3,5.4		
Teaching Learning Process: Quiz/PPT		
UNIT 3:		8 Hours
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures.		
Self-Study Content: Testable Memory Design		
Text book Map: Text 1: 6.1,6.2,6.3,6.4		
Teaching Learning Process: Think Pair share- peer teaching		
UNIT 4:		8 Hours
An Invitation to Design Verification: What is design verification? The basic verification principle, Verification methodology, Simulation-based verification versus formal verification, Limitations of formal verification, A quick overview of Verilog scheduling and execution semantics. **Coding for Verification:** Functional correctness, Timing correctness.		
Self-Study Content: Simulation Performance, Portability and Maintainability		
Text book Map: Text 2: 1.1-1.6, 2.1,2.2		
Teaching Learning Process: Seminar		

UNIT 5:	8 Hours
Simulator Architectures and Operations: The compilers, The simulators, Simulator taxonomy and comparison, Simulator operations and applications.	
Self-Study Content: Incremental Compilation	
Text book Map: Text 2: 3.1, 3.2, 3.3, 3.4	
Teaching Learning Process: Seminar/PPT	
Course Outcomes: At the end of the course students should be able to :	
CO1: Analyze the Digital circuits for testability using fault models, BIST and LFSR for possible test patterns CO2: Generate test vectors or test patterns for testing given combinational or sequential logic circuit CO3: Design built-in self-test for given digital circuit CO4: Articulate the concepts of verification and devise the code to verify the function of given Digital Circuit CO5: For a given topic on DFT/verification conduct literature survey, write and submit a report also make a presentation	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Digital Circuit Testing and Testability	Lala Parag K	1997, 1st Edition	ISBN-13: 978-0-12-434330-6, ISBN: 0-12-434330-9
2	Hardware Design Verification: Simulation and Formal Method Based Approaches	William K.Lam	2005	ISBN: 0-13-143347-4
Reference Books:				
1.	Digital Systems Testing and Testable Design and Friedman A D	Abramovici M, Breuer M A,	1994	
2.	Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits	Vishwani D Agarwal	2002	ISBN: 0-7923-7991-8

Web links and Video Lectures (e-resources)
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **VLSI Testing and Verification**		
Course Code: **P24MECE22**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Using the fault models **analyze** the Digital circuits for testability , BIST and LFSR for possible test patterns	L4	PO1
CO2: Generate test vectors or test patterns for testing given combinational or sequential logic circuit and write a report on test coverage.	L6	PO1, PO2
CO3: Design built-in self-test for the given digital circuit.	L6	PO1
CO4: Articulate the concepts of verification and devise the code to verify the function of given Digital Circuit. Review latest developments in testing and verification and submit a report.	L3,L6	PO1, PO3
CO5: For a given topic on DFT/verification conduct literature survey, write and submit a report also make a presentation.	L4, L6	PO4, PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2	2	2				2	2
CO3	2						
CO4	2		2			2	
CO5				2	2	2	

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **ARM Cortex-M3 and M4 Processors**		
Course Code: **P24MECE23**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
1. Digital design. 2. Microcontroller architecture and programming. 3. Computer organization.		
Course learning Objectives:		
CLO1: To study architecture and basics of ARM Cortex-M3/M4 processors. CLO2: To Develop assembly-level and Embedded C programs and interface with other External Devices. CLO3: To study software development for systems based on Cortex-M3/M4 Processor.		
UNIT -1		8 Hours
Introduction to ARM Cortex-M Processors: Introduction, Advantages and Applications to Cortex - M processors, Resources for using ARM processors and ARM Microcontrollers, Background and history of ARM. **Technical Overview:** General information about the Cortex-M3 and Cortex-M4 processors Features of the Cortex-M3 and Cortex-M4 processors.		
Self-Study Content: Understand the concepts of Introduction to Embedded Software Development flow and Software flow.		
Text book Map: Chapter 1 and Chapter 3.		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 2:		8 Hours
Architecture: Introduction to the architecture, Programmer's model, Behaviour of the application program status register (APSR), Memory system, Exceptions and interrupts, System control block (SCB), Debug, Reset and reset sequence. **Instruction Set:** Background to the instruction set in ARM Cortex-M processors, Comparison of the instruction set in ARM Cortex-M processors, Understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly language (UAL).		
Self-Study Content: Learn Data types in C programming, Inputs-outputs and peripherals accesses for Embedded Software Development.		
Text book Map: Chapter 4 and Chapter 5 (5.1 - 5.5).		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 3:		8 Hours
Instruction Set: Instruction Set, Cortex-M4 specific instructions, Barrel shifter, Accessing special instructions and special registers in programming		
Self-Study Content: Study and present the journal paper "Liu, H. (2023). ARM-Based Embedded System Platform and Its Portability Research. *Journal of Computer and Communications*, *11*(11), 51-63" with DOI: https://doi.org/10.4236/jcc.2023.1111003		
Text book Map: Chapter 5 (5.6 - 5.9).		
Teaching Learning Process: Individual Presentation on the assigned topic.		
UNIT 4:		8 Hours
Memory System: Overview of memory system features, Memory map, Connecting the processor to memory and peripherals, Memory requirements, Memory endianness, Data alignment and unaligned data access support, Default memory access permissions, Memory		

access attributes.

Exceptions and Interrupts: Overview of exceptions and interrupts, Exception types, Overview of interrupt management, Definitions of priority, Vector table and vector table relocation, Interrupt inputs and pending behaviours, Exception sequence overview, Details of NVIC registers for interrupt control, Details of SCB registers for exception and interrupt control.

Self-Study Content: Study Bit-band operations and Memory system in a microcontroller.

Text book Map: Chapter 6 (6.1 – 6.6, 6.8, 6.9) and Chapter 7 (7.1 – 7.9).

Teaching Learning Process: Power point presentation, group discussion, chalk and talk,

UNIT 5: 8 Hours

Exceptions and Interrupts: Details of special registers for exception or interrupt masking, Example procedures in setting up interrupts, Software interrupts.

Low Power and System Control Features: Low power designs, Low power features, Using WFI and WFE instructions in programming, Developing low power applications, The SysTick timer, Self-reset, CPU ID base register, Configuration control register, Auxiliary control register, Co-processor access control register.

Self-Study Content: Study and present the journal paper "Oyetoke, O. O. (2017). A practical application of ARM cortex-M3 processor core in embedded system engineering. *International Journal of Intelligent Systems and Applications*, *9*(7), 70" with DOI: https://doi.org/10.5815/ijisa.2017.07.08

Text book Map: Chapter 7 (7.10 – 7.12) and Chapter 9.

Teaching Learning Process: Individual Presentation on the assigned topic.

Course Outcomes: At the end of the course students should be able to :

CO1: Sketch the architecture of ARM Cortex-M3/M4 processor and illustrate the, modes of operation, instruction set architecture, memory organization and interrupts.
CO2: Illustrate interrupt mechanism with related registers details.
CO3: Analyze the given assembly/Embedded C code for ARM Cortex-M3/M4 and summarize the findings.
CO4: Develop assembly/embedded C code for given function/application specifications.
CO5: Demonstrate and present a summary/report on peripheral interfacing with advanced programming of ARM Cortex M3/M4 microcontrollers for real-time applications.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors	Joseph Yiu	2014 & 3rd Edition	Newnes Publication
2				

Reference Books:

1.	ARM System-on-Chip Architecture	S. Furber	2000 & 2nd Edition	Wesley Publication
2.	Microcontroller-Theory & Applications	A. Deshmukh	2017	Tata McGraw Hill Publication

Web links and Video Lectures (e-resources)

1. ARM Architecture Fundamentals:
https://www.youtube.com/watch?v=7LqPJGnBPMM
2. ARM Instruction Set:
https://www.youtube.com/@IITKharagpurJuly-is9ie
3. Learn Embedded Systems Design on ARM based Microcontrollers:
https://youtu.be/MfhTBeaDpQA

4. ARM Cortex-M3 Processor: https://youtu.be/njjP6sdkqgM
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **ARM Cortex-M3 and M4 Processors**		
Course Code: **P24MECE23**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Sketch the architecture of ARM Cortex-M3/M4 processor and illustrate the, modes of operation, instruction set architecture, memory organization and interrupts.	L3	PO1
CO2: Illustrate interrupt mechanism with related registers details.	L3	PO1
CO3: Analyze the given assembly/Embedded C code for ARM Cortex-M3/M4 and summarize the findings.	L4	PO2
CO4: Develop assembly/embedded C code for given function/application specifications.	L5	PO3
CO5: Demonstrate and present a summary/report on peripheral interfacing with advanced programming of ARM Cortex M3/M4 microcontrollers for real-time applications.	L4	PO4,PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	3					3	
CO3		2					2
CO4			2				
CO5				2	2		

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Real Time Operating Systems**		
Course Code: **P24MECE24**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
• Knowledge of Computer Organization and Architecture. • Understanding of Embedded Systems. • Overview of the operating systems.		
Course learning Objectives:		
CLO1: Understand the concept of a real time system and their implementation. CLO2: To gain knowledge of resource and memory management. CLO3: Understand the role of process and threads in real time systems. CLO4: To introduce firmware and debugging components in RTOS.		
UNIT -1		8 Hours
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions.		
Self-Study Content: Thread Safe Reentrant Functions.		
Text book Map: **Text 1**: Chapter 1 and 2.		
Teaching Learning Process: PPT/Flipped Classroom		
UNIT 2:		8 Hours
Processing with Real Time Scheduling: Pre-emptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline–Monotonic Policy, Dynamic priority policies.		
Self-Study Content: Alternative to RM policy		
Text book Map: **Text 1**: Chapter 2, 3,7.		
Teaching Learning Process: Seminar		
UNIT 3:		8 Hours
Memory and I/O Resources: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi resource Services, Blocking, Deadlock and livelock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences.		
Self-Study Content: Reliable software, Available software.		
Text book Map: **Text 1**: Chapter 4, 5,6,7,11.		
Teaching Learning Process: Seminar/ Simulation		
UNIT 4:		8 Hours
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. **Debugging Components**: Exceptions, assert, checking return codes, Single-step debugging, Test access ports, Trace Ports.		
Self-Study Content: Power-On Self-Test and Diagnostics, External Test Equipment, Application-Level Debugging.		
Text book Map: **Text 1:** Chapter 8 and 9.		

Teaching Learning Process: Group discussion with Case study/ Flipped Classroom

UNIT 5: 8 Hours

Process and Threads: Mutex, Mailboxes, Shell Programming, Process and Thread creations, Multithreading, Programs related to semaphores, Shared Memory, Message queue.

Self-Study Content: Shared Buffer applications involving inter task /thread communication.

Text book Map: **Text 2:** Chapter 7.5, 7.6, 11.2, 11.3.

Teaching Learning Process: PPT/ Chalk and Talk/ Seminar

Course Outcomes: At the end of the course students should be able to :

CO1: Describe the real time operating system concepts, real time service utilities, debugging methodologies and optimization techniques.
CO2: Apply appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/ FPGA/ ASIC) to improve the system performance.
CO3: Real time operating system applications using modern tools.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	"Real-Time Embedded Systems and Components"	Sam Siewert	Cengage Learning India Edition, 2007	
2	"Embedded/ Real Time Systems, Concepts, Design and Programming"	Dr. K.V.K.K Prasad	New edition, 2010	Dream Tech Press

Reference Books:

1.	"Real Time Systems"	Jane W S Liu	2008	Pearson education
2.	"Embedded System Design- An Introduction to Processes, Tools and Techniques"	Arnold S Berger	2002	CMP Books

Web links and Video Lectures (e-resources)

1. https://www.youtube.com/watch?v=dHsHP9RrXBw&list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme: P24
Course Title: **Real Time Operating Systems**		
Course Code: **P24MECE24**	CIE Marks:50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40 hrs	Exam Hours: 03(Theory)	Credits: 03

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Describe the real time operating system concepts, real time service utilities, debugging methodologies and optimization techniques	Understanding and Apply	L2 (PO1)
CO2: Apply appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/ FPGA/ ASIC), priority based static and dynamic real time scheduling techniques to improve the system performance.	Apply	L2 (PO1)
CO3: Real time operating system applications using modern tools.	Create	L3 (PO2, PO3, PO4, PO5)

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	2					2	
CO3		2	1	1	1		2

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Fin FETs and Other Multi-Gate Transistors**		
Course Code: **P24MECE251**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
CMOS VLSI (Analog and Digital), Digital Electronics		
Course learning Objectives:		
CLO1: To learn the evolution of SOI MOS transistor. CLO2: To have an insight into thin film formation techniques and advanced gate stack deposition. CLO3: To enable the students to understand the physics of BSIM-CMG models. CLO4: To analyse the electrical characteristics of the multi-gate MOS system. CLO5: To realise the inter relationship between the multi-gate FET device properties and digital and analog circuits		
UNIT -1		8 Hours
The SOI MOSFET: From Single Gate to Multi-Gate: A brief history of Multiple-Gate MOSFETs, Multi Gate MOSFET physics.		
Self-Study Content: MOSFET scaling and Moore's law, Short-Channel Effects		
Text book Map: Text1- 1.4, 1.5		
Teaching Learning Process:		
UNIT 2:		8 Hours
Multi-gate MOSFET Technology: Introduction, Active Area: Fins, Gate Stack		
Self-Study Content: Source/Drain Resistance and Capacitance, Mobility and Strain Engineering		
Text book Map: Text1-2.1-2.3		
Teaching Learning Process:		
UNIT 3:		8 Hours
BSIM-CMG: A Compact Model for Mult-Gate Transistors: Introduction, Framework for Multi-Gate FET Modeling, Multi-Gate Models, BSIM-CMG and BSIM-IMG, BSIM-CMG.		
Self-Study Content: The BSIM-IMG Model		
Text book Map: Text1-3.1-3.4		
Teaching Learning Process:		
UNIT 4:		8 Hours
Physics of the MultiGate MOS system: Device electrostatics, Double gate MOS system, Two-dimensional confinement		
Self-Study Content: Double-Gate MOSFETs and FinFETs.		
Text book Map: Text1-4.1-4.3		
Teaching Learning Process:		
UNIT 5:		8 Hours
Multi-Gate MOSFET circuit Design: Introduction, Digital Circuit Design, Analog Circuit Design (mixed and RF circuit not included)		
Self-Study Content: Mixed-signal aspects, RF circuit design		
Text book Map: Text1-7.1-7.3.2		
Teaching Learning Process:		

Course Outcomes: At the end of the course students should be able to :

CO1: Illustrate the working principle of FinFETs and multigate transistors with required structure and equations.
CO2: Analyze the circuits involving FinFETS and multigate devices with quantum effects and write a summary
CO3: Design FinFET based analog and digital circuits
CO4: Simulate the electrical and physical characteristics of the FinFET models along with multigate transistors

1.	Title	Author	Year & Edition	Publisher
1	FinFETs and other Multi-Gate Transistors	J. P. Colinge	2008	springer
2				

Reference Books:

1.	FinFET Modeling for IC Simulation and Design: using the BSIM-CMG standard	Yogesh Singh Chauhan, Darsen D	2015	Academic Press
2.	Toward Quantum FinFET	Weihua Han, Zhiming M. Wang	2021 First Edition	Springer Cham,
3.	FinFET Devices for VLSI Circuits and Systems	Samar Saha	2020 First Edition	CRC Press

Web links and Video Lectures (e-resources)

1. http://www.ee.iitb.ac.in
2. http://onlinecourses.nptel.ac.in
3. http;//icmaskdesign.com
4. http;//link.springer.com

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **Fin FETs and Other Multi-Gate Transistors**		
Course Code: **P24MECE251**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Illustrate the impact of physical parameters of the FinFETS and multigate transistors on their electrical behaviour	L4	PO1
CO2: Analyze the circuits involving FinFETS and multigate devices with quantum effects and write a summary	L4	PO1, PO3
CO3: Design FinFET based analog and digital circuits	L5	PO1
CO4: Simulate the electrical and physical characteristics of the FinFET models along with multigate transistors	L5	PO1,PO2

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	3		2			3	
CO3	2					2	
CO4	2	2				2	2
CO5							

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Hardware Security**		
Course Code: **P24MECE252**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite: 1. Basic VLSI Design 2. Digital Electronics and Logic Design 3. Fundamentals of Discrete Mathematics and Algebra		
Course learning Objectives: CLO1: To understand the current practice of SoC design and validation methodology. CLO2: To understand the Security assets and attack models. CLO3: To learn the detection of hardware Trojans in Ips CLO4: To understand the Applications of PUFs		
UNIT -1		8 Hours
Introduction: Mathematical Background: Modular Arithmetic, Groups, Rings, and Fields, Greatest Common Divisors and Multiplicative Inverse, Subgroups, Subrings, and Extensions Groups. Rings, and Field Isomorphisms, Polynomials and Fields, Construction of Galois Field, Extensions of Fields, Cyclic Groups of Group Elements, Efficient Galois Fields, Mapping between Binary and Composite Fields Overview of Modern Cryptography: Introduction, Cryptography: Some Technical Details, Block Ciphers, The AES Round Transformations, Rijndael in Composite Field, Elliptic Curves, Scalar Multiplications: LSB First and MSB First Approaches, Montgomery's Algorithm for Scalar Multiplication		
Self-Study Content: Difference between AES and DES		
Text book Map: Chapter 1 and Chapter 2- Text 1		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 2:		8 Hours
Security and Trust Vulnerabilities in Third-Party IPs: Design and Validation of SoCs, Security and Trust Vulnerabilities in Third-Party IPs, Trustworthy SoC Design Using Untrusted Ips.		
Self-Study Content:		
Text book Map: Chapter 1- Text 2		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 3:		8 Hours
Security Rule Check: Introduction, Security Assets and Attack Models, DSeRC: Design Security Rule Check ,Development of DSeRC Framework		
Self-Study Content:		
Text book Map: Chapter 2- Text 2		
Teaching Learning Process: Individual Presentation on the assigned topic.		
UNIT 4:		8 Hours
Overview of Hardware Trojans: Introduction, Trojan Taxonomy and Examples, Multi-level Attacks, Effect of Hardware Trojan on Circuit Reliability, Hardware Trojan Insertion by Direct Modification of FPGA Configuration Bitstream Code Coverage Analysis for IP Trust Verification, Hardware Trojan Structure, Related Work, A Case Study for IP Trust Verification, Simulation Results		
Self-Study Content: Statistical Approach for Trojan Detection.		

Text book Map: Chapter 13- Text 1, Chapter 4- Text 2

Teaching Learning Process: Power point presentation, group discussion, chalk and talk,

UNIT 5: 8 Hours

Physically Unclonable Functions : Introduction, Classification of PUFs, Realization of Silicon PUFs, Performance Metrics for Quality valuation, Secure PUF: What Makes a PUF Secure, Applications of PUF as a Root-of-Trust, Attacks Model: How PUF Security Could Be Compromised, Looking Forward: What Lies Ahead for PUFs?

Self-Study Content: Genetic Programming based Model building Attack in PUFs

Text book Map: Chapter 18 (text 1)

Teaching Learning Process: Individual Presentation on the assigned topic.

Course Outcomes: At the end of the course students should be able to :

CO1: To Understand and apply fundamental concepts of algebraic structures (groups, rings, fields, and Galois fields), cryptographic algorithms (AES, elliptic curve cryptography), hardware Trojans, security vulnerabilities, and Physically Unclonable Functions (PUFs) in the context of hardware security.

CO2: To Apply cryptographic principles and security rule-checking methodologies (DSeRC framework) to identify and analyze vulnerabilities in System-on-Chip (SoC) designs and third-party IP integrations.

CO3: To Develop advanced security assessment frameworks, utilizing both analytical and simulation-based methods, to ensure hardware reliability and trustworthiness, with emphasis on effective countermeasures against security threats in practical hardware environments.

CO4: To Critically evaluate hardware designs and IP cores by performing comprehensive security assessments to detect, measure, and counteract hardware Trojans, side-channel vulnerabilities, and trust issues in third-party components

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	HARDWARE SECURITY Design, Threats, and Safeguards	Debdeep Mukhopadhyay Rajat Subhra Chakraborty	2015	CRC
2	Hardware IP Security and Trust	Prabhat Mishra · Swarup Bhunia Mark Tehranipoor	2017	Springer Publication

Reference Books:

1.	Introduction to Hardware Security and Trust	Mohammad Tehranipoor Cliff Wang	2012	Springer Publication
2.				

Web links and Video Lectures (e-resources)

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Hardware Security**		
Course Code: **P24MECE252**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: To Understand and apply fundamental concepts of algebraic structures (groups, rings, fields, and Galois fields), cryptographic algorithms (AES, elliptic curve cryptography), hardware Trojans, security vulnerabilities, and Physically Unclonable Functions (PUFs) in the context of hardware security.	L2	PO3
CO2: To Apply cryptographic principles and security rule-checking methodologies (DSeRC framework) to identify and analyze vulnerabilities in System-on-Chip (SoC) designs and third-party IP integrations.	L3	PO1,PO2
CO3: To Develop advanced security assessment frameworks, utilizing both analytical and simulation-based methods, to ensure hardware reliability and trustworthiness, with emphasis on effective countermeasures against security threats in practical hardware environments.	L4	PO2
CO4: To Critically evaluate hardware designs and IP cores by performing comprehensive security assessments to detect, measure, and counteract hardware Trojans, side-channel vulnerabilities, and trust issues in third-party components	L3	PO2,PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1			3		1		
CO2	3	2				3	2
CO3		3					3
CO4		2	3				2

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Static Timing Analysis**		
Course Code: **P24MECE253**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite: 1. Embedded Systems. 2. Advanced Microcontroller. 3. ARM Processor.		
Course learning Objectives: CLO1: To understand the STA Environment and concepts. CLO2: To know standard cell library with timing model and delay model. CLO3: To study delay calculations and timing verification concepts of flip-flops.		
UNIT -1		8 Hours
Introduction: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis? Design Flow, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations. **STA Concepts:** CMOS Logic, Modelling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions.		
Self-Study Content: Understanding Timing Paths and Constraints		
Text book Map: Chapter 1 and Chapter 2		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 2:		8 Hours
Standard Cell Library: Pin Capacitance, Timing Modeling, Timing Models–Combinational Cells, Timing Models-Sequential Cells, State-Dependent Models, Interface Timing Model for a Black Box, Advanced Timing Modeling, Power Dissipation Modeling.		
Self-Study Content: Simulating cells under different conditions to understand their timing behaviour.		
Text book Map: Chapter 3		
Teaching Learning Process: Power point presentation, interactive session, chalk and talk.		
UNIT 3:		8 Hours
Interconnect Parasitics: RLC for Interconnect, Wireload Models, Representation of Extracted Parasitics, Representing Coupling Capacitances, Hierarchical Methodology, Reducing Parasitic for Critical Nets. **Delay Calculation:** Overview, Cell Delay using Effective Capacitance, Interconnect Delay, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Slack Calculation		
Self-Study Content: Modelling of parasitic interconnection inductances on the GaAs-based VLSIC's.		
Text book Map: Chapter 4 and Chapter 5		
Teaching Learning Process: Individual Presentation on the assigned topic.		
UNIT 4:		8 Hours
Configuring the STA Environment: What is the STA Environment? Specifying Clocks, Generated Clocks, Constraining Input Paths, Constraining Output Paths, Timing Path Groups, Modeling of External Attributes, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Point-to-Point Specification, Path Segmentation.		

Self-Study Content: STA Fundamentals

Text book Map: Chapter 7

Teaching Learning Process: Power point presentation, group discussion, chalk and talk,

UNIT 5: 8 Hours

Timing Verification: Setup Timing Check, Hold Timing Check, Multi cycle Paths, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Examples, Half-cycle Path-Case1, Half-cycle Path-Case2, Fast to Slow Clock Domain.

Self-Study Content: Multiple Clocks.

Text book Map: Chapter 8

Teaching Learning Process: Individual Presentation on the assigned topic.

Course Outcomes: At the end of the course students should be able to :

CO1: To Understand and apply STA principles for digital circuits.
CO2: To analyse and optimize the static timing analysis for any given digital circuits
CO3: To Design a timing constraint for the given specification.
CO4: Generate the timing analysis report using EDA tool for different checks.
CO5: Analyse the generated report to identify critical issues and bottleneck for the STA violation.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Static Timing Analysis for Nanometer Designs: A Practical Approach	J. Bhasker, R Chadha	2009	Springer Publication
2				

Reference Books:

1.	Constraining Designs for Synthesis and Timing Analysis–A Practical Guide to Synopsis Design Constraints(SDC)	Sridhar Gangadharan, Sanjay Churiwala	2013	Springer Publication
2.	Timing Analysis and Optimization of Sequential Circuits	Naresh Maheshwari and Sachin Sapatnekar	2009	Springer Publication

Web links and Video Lectures (e-resources)

1. https://www.youtube.com/watch?v=KlUn2GjNOfY&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e
2. https://www.youtube.com/watch?v=yYR8BzysTmM&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e&index=2

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Static Timing Analysis**		
Course Code: **P24MECE253**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: To Understand and apply STA principles for digital circuits.	L2	PO1
CO2: To analyse and optimize the static timing analysis for any given digital circuits	L3	PO2
CO3: To Design a timing constraint for the given specification.	L4	PO2
CO4: Generate the timing analysis report using EDA tool for different checks.	L2	PO3,PO5
CO5: Analyse the generated report to identify critical issues and bottleneck for the STA violation.	L3	PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3		3					3
CO4			3		3		
CO5					2		

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Embedded Linux System Design and Development Processing**		
Course Code: **P24MECE254**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
• Microcontroller/Micro Processor and Bus architectures • Digital systems and Memory • Operating System		
Course learning Objectives:		
CLO1: To understand the importance of Embedded Linux in embedded system design. CLO2: To Gain the knowledge of Board Support Package. CLO3: To Analyse the memory requirements for design. CLO4: To learn the embedded drivers and kernel modules. CLO5: To learn the porting applications from traditional RTOS.		
UNIT -1		8 Hours
Introduction: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. Getting Started: Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross Platform Toolchain RBT Levels: L2, L3		
Self-Study Content: Real life and embedded Linux system		
Text book Map: **Text 1**: Chapter 1 and 2.		
Teaching Learning Process: PPT/Flipped Classroom		
UNIT 2:		8 Hours
Board Support Package: Inserting B S Pin Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Sub system, Timers, UART, Power Management. RBT Levels: L2, L3		
Self-Study Content: General purpose networking		
Text book Map: **Text 1**: Chapter 3.		
Teaching Learning Process: Seminar		
UNIT 3:		8 Hours
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash- Mapping Drivers, MTD Block and Character Devices, Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory. RBT Levels: L2, L3		
Self-Study Content: Disk devices		
Text book Map: **Text 1**: Chapter 4.		
Teaching Learning Process: Seminar/ Simulation		
UNIT 4:		8 Hours
Embedded Drivers: Linux Serial Driver, I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules. RBT Levels: L2, L3		
Self-Study Content: Ethernet Driver		
Text book Map: **Text 1:** Chapter 5.		

Teaching Learning Process: Group discussion with Case study/ Flipped Classroom

UNIT 5: 8 Hours

Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

RBT Levels: L2, L3

Self-Study Content: Embedded boot loaders

Text book Map: **Text 2:** Chapter 6.

Teaching Learning Process: PPT/ Chalk and Talk/ Seminar

Course Outcomes: At the end of the course students should be able to :

CO1: Understand the embedded Linux development environment
CO2: Understand and create Linux BSP for a hardware platform.
CO3: Understand the Linux model for embedded storage and write driver sand applications for the same
CO4: Understand various embedded Linux drivers such as serial, I2C, and so on.
CO5: Port applications to embedded Linux from a traditional RTOS.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	"Embedded Linux System Design And Development"	P. Raghavan, AmolLad, Sriram Neelakandan	2006	Auerbach Publications, Taylor& Francis Group,
2	"Building Embedded Linux Systems"	Karim Yaghmour, Jon Masters, Gilad Ben Yossef, and Philippe Gerum		O'Re i llypublications,2ndedition"

Reference Books:

1.				
2.				

Web links and Video Lectures (e-resources)

1. . https://www.youtube.com/watch?v=9vsu67uMcko

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Embedded Linux System Design and Development Processing**		
Course Code: **P24MECE254**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: To understand the Embedded Linux System principles and its architecture	L1	PO1
CO2: To comment on and summarize Embedded storage and drivers	L2	PO1
CO3:.To Interpret and analyse the functions of Embedded Linux Kernel and drivers	L2	PO2
CO4: To illustrate the bus architectures, drivers and Kernel modules	L2	PO1
CO5: To comprehend the Embedded Linux system packages and porting of applications	L1	PO2

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	3					3	
CO3		2					2
CO4	2					2	
CO5		2					2

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Reconfigurable Computing**		
Course Code: **P24MECE261**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P):	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
FPGA, Verilog HDL, Signal Processing, Image processing		
Course learning Objectives:		
CLO1: To learn the various Reconfigurable systems. CLO2: To study the different Languages and Compilation. CLO3: To understand the Implementation of FPGA. CLO4: To learn Partial Reconfiguration Design. CLO5: To understand the Signal Processing Applications.		
UNIT -1		8 Hours
Introduction: History, Reconfigurable vs. Processor based system, RC Architecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. **Reconfigurable Computing System:** Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System.		
Self-Study Content: Programs on FPGA		
Text book Map: Text 1: 1.1,1.2,2.1,2.2,3.1,3.2		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
Languages and Compilation: Design Cycle, Languages - HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.		
Self-Study Content: Algorithmic RC Languages		
Text book Map: Text 1: 4.1,4.2.2,4.3,4.4,4.5		
Teaching Learning Process: Team Demonstration		
UNIT 3:		8 Hours
Implementation: Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices**: Modelling, Temporal Partitioning Algorithms.		
Self-Study Content: Developing a different design flow to study FPGA.		
Text book Map: Text 2 : 3.1,3.2,3.3,4.1,4.2		
Teaching Learning Process: Poster Presentation		
UNIT 4:		8 Hours
Partial Reconfiguration Design: Partial Reconfiguration Design, Bit stream Manipulation with J Bits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.		
Self-Study Content:		
Text book Map: Text 2: 7.1.7.2,7.3,7.,4,7.5,7.6,7.7		
Teaching Learning Process: Case study		
UNIT 5:		8 Hours
Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beam forming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. **System on a Programmable Chip:** Introduction to SoPC, Adaptive Multiprocessing on		

Chip.

Self-Study Content: i) Morphology
ii) Feature Extraction
iii) Image Matching

Text book Map: Text 1: 5.2.1, 5.3,5.4.1, 5.4.2, 6.1, 6.2, 6.3
Text 2: 8.1,8.2,8.3

Teaching Learning Process: Seminar

Course Outcomes: At the end of the course students should be able to :

CO1: Understand the fundamental principles and practices in reconfigurable architecture.
CO2: Apply simulation and synthesize of reconfigurable computing architectures.
CO3: Analyze the FPGA design principles, and logic synthesis.
CO4: Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
CO5: Design digital systems for a variety of applications on signal processing and system on chip configurations.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays	Maya B. Gokhale and Paul S. Graham	2005 ISBN:978-0-387-26105-82005	Springer
2	Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications.	Christophe Bobda	ISBN:978-1-4020-6088-52007	Kluwer Academic

Reference Books:

1.	Practical FPGA Programming in C	D. Pellerin and S. Thibault	2005	Prentice-Hall
2.	FPGA Based System Design	W.Wolf	2005	Prentice-Hall
3.	Rapid System Prototyping with FPGAs: Accelerating the Design Process	R.Cofer and B.Harding Newnes	2005	

Web links and Video Lectures (e-resources)

1. https://www.youtube.com/watch?v=q2ZbxPFtowM
2. https://youtu.be/5_H_j72Ftq8?si=kqiNA07iUBwKRtNP
3. https://nptel.ac.in/courses/117108040

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Reconfigurable Computing**		
Course Code: **P24MECE261**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Understand the fundamental principles and practices in reconfigurable architecture	L2	PO1
CO2: Analyze the simulation and synthesize of reconfigurable computing architectures	L3	PO2
CO3: Analyze the FPGA design principles, and logic synthesis.	L2,L3	PO2,PO3
CO4: Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.	L4	PO3
CO5: Design digital systems for a variety of applications on signal processing and system on chip configurations.	L6	PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2		3					3
CO3		3					3
CO4			2				
CO5					2		

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Long Term Reliability of VLSI Systems**		
Course Code: **P24MECE262**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite: 1. Design and Analysis of CMOS Circuits 2. Knowledge on Device-level Modelling 3. Familiarity with Circuit Simulation Tools 4. Knowledge on Fabrication Technology		
Course learning Objectives:		
CLO1: To Understand the Various Concepts Related to Electro migration Reliability. CLO2: To study the Fast EM Stress Evolution Analysis. CLO3: To study the EM Assessment for Power Grid Networks. CLO4: To understand the Transistor Aging Effects and Reliability. CLO5: To learn the Aging Effects in Sequential Elements.		
UNIT -1		8 Hours
Electro migration Reliability: Why Electro migration Reliability?, Why system level EM Reliability Management? Physics- based EM Modelling, Electro migration Fundamentals, Stress based EM Modelling and stress diffusion equations, Modelling for transient EM effects and Initial stress conditions, post voiding stress and void volume evolution, compact physics based EM model for a single wire, other relevant EM models and analysis methods.		
Self-Study Content: Study on recent developments in EM topics		
Text book Map: 1.1,1.2,2.1,2.2,2.3,2.4,2.5,2.6,2.9		
Teaching Learning Process: One minute paper, Quiz		
UNIT 2:		8 Hours
Fast EM Stress Evolution Analysis: Introduction, The LTI ordinary differential equations for EM stress evolution, The presented Krylov fast EM stress analysis, Numerical results and discussions.		
Self-Study Content: Understand Krylov subspace method		
Text book Map: 3.1,3.2,3.3,3.4		
Teaching Learning Process: Presentations		
UNIT 3:		8 Hours
EM Assessment for Power Grid Networks: New power grid reliability analysis method, cross-layout temperature and thermal stress characterization, impact of across-layout temperature and thermal stress on EM.		
Self-Study Content: Implement full chip thermal variation aware EM assessment method on a 2.4ghz Linux server using C++. Test the same using 32nm standard cell IC design.		
Text book Map:7.2,7.4,7.5		
Teaching Learning Process: Quiz, Presentation		
UNIT 4:		8 Hours
Transistor Aging Effects and Reliability: Introduction, Transistor reliability in advanced technology nodes, Transistor Aging, BTI-Bias Temperature Instability, HCI–Hot Carrier Injection, Coupling models for BTI and HCI degradations, RTN–Random Telegraph Noise, TDDB–Time Dependent Dielectric Breakdown.		
Self-Study Content: Understand various modelling and mitigation techniques for transistor aging at various levels of abstraction.		
Text book Map: 13.1,13.2		

Teaching Learning Process: Quiz, Presentation

UNIT 5:	8 Hours

Aging Effects in Sequential Elements: Introduction, Background: flip flop timing analysis, process variation model, voltage droop model, Robustness analysis, reliability-aware flip-flop design.

Self-Study Content: Perform layout simulation of C2MOS Flip-flop using Cadence Virtuoso.

Text book Map: 16.1,16.2,16.3,16.4

Teaching Learning Process: Quiz ,Presentation

Course Outcomes: At the end of the course students should be able to :

CO1: Comprehend the recent research in the area of interconnect and device reliability.
CO2: Understand the physics-based EM modelling.
CO3: Understand the underlying phenomena of BTI, HCI, TDDB leading to device
CO4: Relate to considerations at the circuit-level with both combinational and sequentialL4elements

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Long- Term Reliability of Nanometer VLSI Systems	SheldonX.D.Tan, Mehdi Baradaran Tahoori, Taeyoung Kim, SamanKia mehr, Zeyu	1stEdition,2019ISBN:978-3-030-26171-9	Springer International Publishing
2				

Reference Books:

1.	Reliability Wearout Mechanisms in Advanced CMOS Technologies	Alvin Wayne Strong, Rolf-Peter Vollertsen, Timothy D. Sullivan, Ernest Y. Wu, Giuseppe La Rosa, Jordi Sune	Inc.2009Print ISBN:9780471731726	Wiley, Copyright © the Institute of Electrical and Electronics Engineers
2.	Hot- carrier Reliability of MOS VLSI Circuits	Yusuf Leblebici, SM Kang	1stEdition , 1993	Springer Science & Business Media
3	Fundamentals of Electromigration Aware Integrated Circuit Design	Matthias Thiele, Jens Lienig Springer International Publishing 2018	2018	Springer International Publishing

Web links and Video Lectures (e-resources)

1. nptel.ac.in

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Long Term Reliability of VLSI Systems**		
Course Code: **P24MECE262**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Comprehend the recent research in the area of interconnect and device reliability.	L2	PO1
CO2: Understand the physics-based EM modelling.	L2	PO2
CO3: Understand the underlying phenomena of BTI, HCI, TDDB leading to device	L2	PO2
CO4: Relate to considerations at the circuit-level with both combinational and sequentialL4elements	L4	PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3		2					2
CO4			1				

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **Low Power VLSI Design**		
Course Code: **P24MECE263**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite: 1. Digital Electronic Circuits. 2. Digital CMOS VLSI 3. Circuit Analysis		
Course learning Objectives:		
CLO1: Apply State-of-the art approaches to power estimation and reduction. CLO2: Describe various power reduction and the power estimation methods. CLO3: Understand power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system.		
UNIT -1		8 Hours
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. Simulation power analysis: SPICE circuit simulation, Monte Carlo simulation.		
Self-Study Content: Discrete Transistor Modeling and Analysis, Gate-Level Logic Simulation, Architecture-Level Analysis, and Data Correlation Analysis in DSP Systems using simulation tools and mathematical methods.		
Text book Map: **1.1 to 1.7, 2.1, 2.6 (Text 1)**		
Teaching Learning Process: PPT/chalk and talk, Seminar.		
UNIT 2:		8 Hours
Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.		
Self-Study Content: Special latches and flip-flops, low-power digital cell library.		
Text book Map**: 4.1 to 4.6 (Text 1)**		
Teaching Learning Process: PPT/chalk and talk/simulation.		
UNIT 3:		8 Hours
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution**: Power dissipation in clock distribution, single driver versus distributed buffers.		
Self-Study Content: Gate reorganization, signal gating, logic and state machine encoding, and pre-computation logic.		
Text book Map: **5.1 to 5.5 (Text 1), 5.1 to 5.2 (Text 2)**		
Teaching Learning Process: PPT/chalk and talk /Individual Role play/Team Demonstration.		
UNIT 4:		8 Hours
Low power Architecture and Systems: Power and performance management, switching activity reduction, flow graph transformation. **Low power memory design**: Introduction, sources and reductions of power dissipation in memory subsystem**.**		
Self-Study Content: Sources of Power Dissipation in DRAM and SRAM, Low Power DRAM Circuits and Low Power SRAM Circuits to enhance energy efficiency in memory systems.		

Text book Map: **7.1 to 7.4 (Text 1), 8.1 to 8.2(Text 2).**	
Teaching Learning Process: PPT/chalk and talk / Individual Role play/Team Demonstration.	
UNIT 5:	8 Hours
Algorithm and Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis and optimization, Architectural level estimation and synthesis. Advanced Techniques: Adiabatic computation, Asynchronous circuits.	
Self-Study Content: Pass Transistor Logic Synthesis, Basics of Pass Transistor Logic, Boolean Decision Diagram and Pass Transistor Logic, Pass Transistor Logic Synthesis System.	
Text book Map: **11.1 to 11.5 (Text 2), 8.1, 8.3 (Text 1).**	
Teaching Learning Process: PPT/chalk and talk/Flip class/ Case study.	
Course Outcomes: At the end of the course students should be able to :	
CO1: Identify and illustrate the sources of power dissipation, also formulate and compute the dissipated power at different abstract levels of the circuits. CO2: Analyse the given circuits for the impact of transistor sizing, gate sizing, equivalent pin ordering, network restructuring, and special latches and flip-flops in power consumption reduction. CO3: Apply circuit-level and logic-level design strategies such as transistor sizing, gate sizing, signal gating, logic encoding, and low-power cell design to minimize power consumption. CO4: Design and optimize low-power digital cells using techniques such as adjustable device threshold voltage, gate reorganization, signal gating, and logic encoding. CO5: Apply SPICE circuit simulation and Monte Carlo simulation to analyse and optimize power consumption in VLSI circuits.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Practical Low Power Digital VLSI Design	Gary K.Yeap	1998	ISBN 978-1-4613-7778-8, ISBN 978-1-4615-6065-4, (eBook) DOI 10.1007/978-1-4615-6065-4.
2	Low Power Design Methodologies	Jan M. Rabaey University Califomia and Massoud Pedram University of Southem Califomia	2010	ISBN 978-1-46 13-5975-3, ISBN 978-1-4615-2307-9, (eBook) DOI 10.1007/978-1-4615-2307-9.

Reference Books:

1.	Low-Power CMOS VLSI Circuit Design	Kaushik Roy, Sharat Prasad.	2000	
2.	Low power digital CMOS design.	A.P.Chandrasekaranand, R.W.Broadersen	1995	
3.	Low power VLSI CMOS circuit design.	A Bellamour and MIElmasri	1995	

Web links and Video Lectures (e-resources)

1. https://archive.nptel.ac.in/courses/106/105/106105034/
2.https://www.youtube.com/watch?v=TFOO1JAll2Y
3.https://www.youtube.com/watch?v=ORtlxpW_LMU

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **Low Power VLSI Design**		
Course Code: **P24MECE263**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Illustrate and compare the sources of power dissipation, also formulate and compute the dissipated power at different abstract levels of the circuits.	L3	PO1
CO2: Analyse the given circuits for the impact of transistor sizing, gate sizing, equivalent pin ordering, network restructuring, and special latches and flip-flops in power consumption reduction. Present a seminar on prevalent low power practices in the industry.	L4	PO1, PO4
CO3: Apply circuit-level and logic-level design strategies such as transistor sizing, gate sizing, signal gating, logic encoding, and low-power cell design to minimize power consumption.	L2	PO1
CO4: Design and optimize low-power digital cells using techniques such as adjustable device threshold voltage, gate reorganization, signal gating, and logic encoding.	L6	PO1
CO5: Apply SPICE circuit simulation and Monte Carlo simulation to analyse and optimize power consumption in VLSI circuits and submit a report.	L2	PO6

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	2			1		2	
CO3	2					2	
CO4	2					2	
CO5					2		

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **RISC V**		
Course Code: **P24MECE264**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
Digital Logic Design, Microcontroller, Microprocessor		
Course learning Objectives:		
CLO1: To study the basics of RISC-V architecture. CLO2: To understand the RISC-V Implementation. CLO3: To create the data path in RISC-V.		
UNIT -1		8 Hours
Instructions: Introduction ,Operations of the Computer, Operands of the Computer Hardware, Signed and Unsigned Numbers , Representing Instructions in the Computer, Logical Operations , Instructions for Making Decisions, Supporting Procedures in Computer Hardware, Communicating with People, RISC-V Addressing for Wide Immediate and Addresses.		
Self-Study Content: Real stuff: MIPS Instructions.		
Text book Map: Text1		
Teaching Learning Process: Chalk and Board /Seminar		
UNIT 2:		8 Hours
Instructions continued : Parallelism and Instructions: Synchronization, Translating and Starting a Program, AC Sort Example to Put it All Together, Real Stuff: The Rest of the RISC-V Instruction Set. **Arithmetic for Computers**: Addition and Subtraction, Multiplication, Multiply in RISC-V, Division, Divide in RISC-V, Floating-Point Instructions in RISC-V.		
Self-Study Content: Real stuff: Streaming SIMD Extensions and Advanced Vector.		
Text book Map: Text1		
Teaching Learning Process: Case study		
UNIT 3:		8 Hours
The Processor: A Basic RISC-V Implementation, An Overview of the Implementation, Logic Design Conventions, Building a Data path, A Simple Implementation Scheme, Overview of Pipelining.		
Self-Study Content: Exceptions		
Text book Map: Text1		
Teaching Learning Process: Report writing		
UNIT 4:		8 Hours
The Processor continued: Pipelined Data path and Control, Data Hazards: Forwarding versus Stalling, Control Hazards. How Exceptions are Handled in the RISC-V Architecture, Instruction-Level Parallelism and Matrix Multiply. **Large and Fast:** Exploiting Memory Hierarchy, Memory Technologies.		
Self-Study Content: An Introduction to Digital Design Using a Hardware Design Language to Describe and Model a Pipeline and More Pipelining Illustrations.		
Text book Map: Text1		
Teaching Learning Process: Power point Presentation		
UNIT 5:		8 Hours
Large and Fast: Exploiting Memory Hierarchy continued: The Basics of Caches, Virtual Machines, Virtual Memory.		

Self-Study Content: Going Faster: Cache Blocking and Matrix Multiply.

Text book Map: Text1

Teaching Learning Process: Seminars

Course Outcomes: At the end of the course students should be able to :

CO1: Describe RISC-V instructions and the language of the computer.
CO2: Analyse Data Hazards and how Exceptions are handled in the RISC-V Architecture
CO3: Design using the knowledge of memory mapping techniques..
CO4: Construct a data path and implementation using floating-point arithmetic.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	Computer Organization and Design: The Hardware/Software Interface: RISC-V Edition	David A. Patterson, John L. Hennessy	5th Edition	Elsevier. Morgan Kaufman
2				

Reference Books:

1.	Digital Design and Computer Architecture,	David Money Harris, Sarah L. Harris	2021& RISC-V Edition	Morgan Kaufman
2.	Guide to Computer Processor Architecture: A RISC-V approach, with High-Level Synthesis	Bernard Goossens	2023	Springer

Web links and Video Lectures (e-resources)

1.https://www.youtube.com/watch?v=TVvMPh_P2is&list=PLgzAvj2cYr3qGvecT_PSnKzl5SxECZmI3&index=2,
2.https://www.youtube.com/watch?v=BVvDHhG0RoA&list=PL5AmAh9QoSK7Fwk9vOJu-3VqBng_HjGFc

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **RISC V**		
Course Code: **P24MECE264**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Describe RISC-V instructions and the language of the computer.	L2	PO1
CO2: Analyse Data Hazards and how Exceptions are handled in the RISC-V Architecture.	L3	PO2
CO3: Design using the knowledge of memory mapping techniques.	L3	PO3
CO4: Construct a data path and implementation using floating-point arithmetic.	L3	PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		3					3
CO3			1				
CO4				1			

PART-A		
Academic Year: 2024-25	Semester: II	Scheme: P24
Course Title: **VLSI Design and Embedded Systems Lab**		
Course Code: **P24MECEL27**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 0:1:1	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **02**		
Prerequisite:		
Verilog, Microcontroller.		
Course learning Objectives:		
CLO1: To design and simulate digital circuits: standard cells, ALUs, SRAM cells, and matrix multiplication units. CLO2: To develop embedded code for the ARM Controller. CLO3: To apply programming skills to real-world problems dealing with the digital and analog circuit design, embedded systems, and microcontrollers		

Sl.No.	**Experiments**
	Part-A **VLSI Design**
1	Functional simulation and characterization of a given standard cell.
2	Develop an ALU macro for the given requirements.
3	Design and develop an SRAM cell for the given specification.
4	Develop a matrix multiplication unit for the given specification.
5	Develop analog differentiator for the given specification or requirements.
6	Develop an oscillator for given specification.
	Part-B **Embedded Systems**
1	Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM =10+9+8+.+1
2	Write a Embedded C program to output the “Hello World” message using UART.
3	Develop a Embedded C program i. To operate a buzzer ii. To control stepper motor using CortexM3
4	Develop a Embedded C program to generate PWM (Using the Internal PWM module of ARM controller) and vary its duty cycle.
5	Develop a Embedded C program for interfacing a DAC and generate (Triangular and Square) waveforms.
6	Write an Assembly language program to store data in RAM.

Course Outcomes: At the end of the course students should be able to :
CO1: Develop MOSFET-based circuits for given analog and digital requirements or operation. CO2: Verify and evaluate the operation of a circuit or code. CO3: Design code for the given specification: Assembly, Embedded C and Verilog. CO4: Test and Analyse the code or circuits for functional and performance requirements.

PART-B		
Academic year:2024-25	Semester: II	Scheme:P24
Course Title: **VLSI Design and Embedded Systems Lab**		
Course Code: **P24MECEL27**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 0:1:1	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 02		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Develop analog or digital or mixed mode circuits for given analog or/and digital requirements.	L6	PO1
CO2: Verify and evaluate the operation of a circuit or code.	L5	PO1
CO3: Develop a code for the given specifications: Assembly, Embedded C and Verilog.	L6	PO1,PO3
CO4: Test and Analyse the code or circuit for functional and performance requirements. Write and submit a report on the outcome of testing and analysis.	L4	PO1, PO5, PO6

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2	3					3	
CO3	2		2			2	
CO4	2				2	2	